FINE-GRAIN ON-CHIP POWER MANAGEMENT USING DIGITAL AND DIGITALLY-ASSISTED LINEAR VOLTAGE REGULATORS

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FINE-GRAIN ON-CHIP POWER MANAGEMENT USING DIGITAL AND DIGITALLY-ASSISTED LINEAR VOLTAGE REGULATORS

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The wise statement is the lost property of the believer, so wherever he finds it, then he is more worthy of it

Muhammad(PBUH) - Jamiʿ at-Tirmidhi (Vol. 5, Book 39, Hadith 2687)

I would like to dedicate this thesis to my parents and my wife.

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SUMMARY

Conventional power delivery using bulky off-chip voltage regulator module fails to adequately address the challenges posed on power delivery network by transistor and voltage scaling, increased parasitic effects, decreased decoupling capacitor budget, high power density and heterogeneity of load circuits. To address these challenges, this dissertation research demonstrates that digital and digitally-assisted linear voltage regulators serve as key design enablers for fine-grain power management right at the point of load.

The proposed designs achieve both spatial and fast temporal adaptation of supply voltage needed to achieve unprecedented levels of performance and reduced energy consumption in big multi-core processors and system-on-chip platforms. They provide an opportunity for automated synthesis, desired process and voltage scalability thanks to their digital construction, wide operational dynamic range, low power overhead, and fast response times as compared to the state-of-the-art designs in linear voltage regulation. This dissertation research also provides theoretical models to understand operational dynamics of digital linear voltage regulators and builds a number of test-chips utilizing advance control laws to enable voltage regulation of small digital functional units to large core-sized digital circuits. Digitally-assisted or hybrid linear voltage regulators build further on top of digital linear voltage regulators to enable fine-grain power management for all types of load circuits and not just digital load circuits achieving unprecedented levels of efficiency and performance.

The designs covered in this thesis have significantly contributed towards understanding the operation and design of digital and digitally-assisted linear voltage regulators. These designs have helped in improving state-of-the-art in on-chip voltage regulation and enabled adoption of digital linear voltage regulators in commercial products.

CHAPTER 1
INTRODUCTION

Increasing performance and energy-efficiency requirements in big multi-core processors and System-on-Chip (SoC), designed in scaled CMOS transistor nodes, pose serious challenges to the effectiveness of existing power delivery and management techniques [1, 2, 3, 4]. As the operational voltage drops down to enable quadratic gains in power ($P = CV^2F$), the higher current passing through the power delivery network (PDN) magnifies the power losses due to board, package and chip parasitics [5]. Similarly, with decreasing transistor and routing metal geometries, increasing process variations and decreasing decoupling capacitor budget, ensuring power supply integrity and accuracy at the Point-of-Load (PoL) becomes difficult [6].

This power delivery problem is further exacerbated by the fact that most of the underlying circuits in these big chips are highly heterogeneous in nature and demand different voltage levels for optimal energy-performance trade-off [7, 8]. These heterogeneous circuits can be broadly classified in to digital and analog circuits. Digital circuits exhibit large dynamic range across current (nA to A) and voltage (V_{MAX} down to transistor threshold voltage). Therefore, metrics like low voltage operation, fast transient response to load current step changes, dynamic scaling of supply voltage (DVS) and instantaneous power state transitions under different performance modes assume prime importance in digital circuits [1]. Analog circuits, on the other hand, require high rejection against power supply noise and precise voltage levels. [9].

To address all these aforementioned challenges due to scaling and load circuits heterogeneity, fine-grain power management right at the PoL has become necessary [6, 10]. Not only multiple voltage levels have to be distributed across the whole chip but they also need to change in time across different sections of the chip to ensure high energy efficiency. To

serve this end, this dissertation research proposes digital and digitally-assisted linear voltage regulators (LVR) as the circuit building blocks for achieving fine-grain spatio-temporal on-chip power delivery and management.

Linear CMOS voltage regulators operated in low dropout (LDO) mode serve as the candidate of choice for PoL power management as opposed to other available DC-DC power converter topologies namely, switched capacitor (SCVR) and inductor (typically referred to as Integrated Voltage Regulator or IVR) based voltage converters. This is because an LDO offers easier on-die integration since it only requires active devices and no passive components to down-convert voltage. It offers process and voltage scalability, small silicon area overhead, high rejection capability against power supply noise and faster response times to load current changes as compared to SCVR and IVR designs [11, 12]. On the downside, linear voltage regulators are lossy by definition as opposed to SCVR and IVR power converters but their power losses are easily offset by the system-level gains achieved through distributing multiple LDOs right at the PoL. This fine-grain integration of LDOs right next to the load has resulted in unprecedented levels of energy-performance trade-offs as shown in recent commercial big-chip designs [13, 3].

1.1 Linear Voltage Regulation: Basic Structure and Terminology

Linear voltage regulation uses active devices like transistors for down conversion of supply voltage. If the difference between the down converted (V_{REG}) and supply voltage (V_{IN}) (called dropout voltage) is on the order of few hundreds of mV then linear voltage regulators are called low dropout voltage regulators or LDO in short. Linear voltage regulation is inherently a lossy voltage down conversion process as the energy is not stored in any passive device like a capacitor or inductor during this conversion. The power conversion efficiency of an LDO is directly proportional to its dropout voltage. Assuming negligible

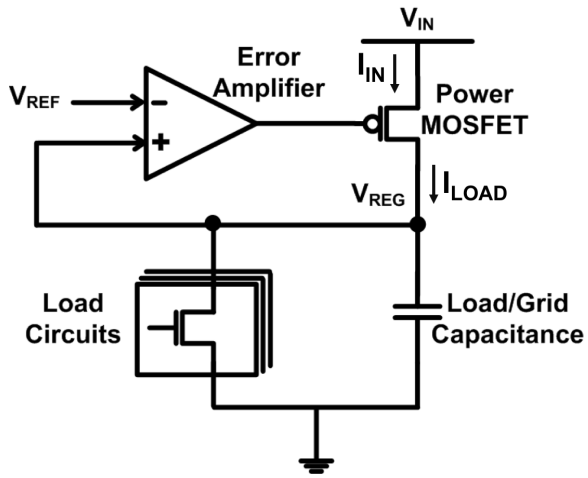


Figure 1.1: Basic structure of an analog LDO.

current consumption in the control circuitry, it is given as

$$P_{EFF} = (I_{LOAD} * V_{REG}/I_{IN} * V_{IN}) * 100 = (V_{REG}/V_{IN})\% \tag{1.1}$$

Here V_{IN} is the supply voltage, V_{REG} is the regulated output voltage of the LDO, I_{IN} is the current drawn from the supply and I_{LOAD} is the current delivered to the load. P_{EFF} expression results from the fact that I_{LOAD}=I_{IN} while only the voltage is down-converted.

The basic bare-bone structure of a conventional analog LDO is shown in fig. 1.1. It implements negative feedback to achieve down-conversion and regulation. An error amplifier or a transconductance stage amplifies the difference between the regulated (V_{REG}) and reference voltages (V_{REF}). This amplified signal controls the gate of a large power transistor to increase or decrease the current delivered to the load circuit modulating V_{REG}. Typically, this power stage employs a P-type power MOSFET to achieve very low dropout voltages. If $V_{REG}>V_{REF}$, V_G increases to bring down V_{REG} and decreases when $V_{REG}<V_{REF}$. V_{REF} is typically generated through a band-gap voltage reference or an external source. The accuracy and bandwidth of this regulation action is dictated by the gain and the most dominant pole of this second order feedback system. Analog LDOs either have the dominant poles on one of the internal nodes of the loop (like V_G) or on the output (V_{REG}) and as such they

are referred to as internal pole dominant LDO or output pole dominant LDO, respectively. Given that there is a limited budget for integration of passives on silicon, internal pole dominant LDOs are typically built for on-chip applications with minimum possible decoupling capacitor budget satisfying the stability constraints of the second order feedback loop.

The metrics which are used to characterize the effectiveness of an LDO are as follows. Load regulation is defined as the ability of the LDO to maintain voltage regulation accuracy across the complete I_{LOAD} range. Line Regulation refers to the maintenance of V_{REG} under DC changes on V_{IN}. Power supply noise rejection (PSR) is the noise rejection capacity of an LDO to prevent any changes on V_{REG} under AC perturbations on V_{IN}. Transient response and voltage droop mitigation capability of an LDO refers to the ability of an LDO to quickly limit the magnitude of voltage drop (incurred due to parasitic resistance and inductor in the current path under a sudden change in load current) and recover to the desired voltage level under a large load current step on V_{REG}. Current efficiency of an LDO is defined as

$$I_{EFF} = (1 - I_{CNTL}/I_{LOAD})\% \tag{1.2}$$

Here, I_{CNTL} refers to the controller current consumption during regulation and I_{LOAD} is the current delivered to the load. A higher current efficiency brings an LDO closer to its theoretical power efficiency limit. Usually a figure of merit (FoM) for an LDO incorporates all these metrics in one form or the other [14]. In the following chapters, we will define a relevant FoM used to gauge the effectiveness of each LDO in addition to all the above-mentioned basic metrics.

1.2 Limitations of Conventional Designs

Analog LDOs exhibiting high current efficiency, fast small-signal response and high PSR continue to be explored to provide on-chip voltage regulation [15, 14, 16, 17]. However, with decreasing supply voltages, the bandwidth and performance of analog LDOs continue

to decrease. Not only the design has become increasingly difficult to achieve a large operational range both in current and voltage but also the nature of the underlying load has changed.

Traditionally, analog LDOs have been employed for voltage sensitive analog load circuits, which typically represent DC loads [9]. Digital load circuits, on the other hand, exhibit large load transients and wide operating voltages [1]. Hence, LDOs that supply digital loads have a different value proposition, such as the capacity to operate across wide operating voltages and respond to instantaneous large load current steps. This is particularly true when the underlying load circuit is in a low-current/low-power state and needs to wake up in a few clock cycles [1]. Other conventional metrics of analog LDOs, like voltage ripple and PSR can be relaxed as these non-idealities are accounted for in digital load circuits by adding a small margin to the already existing voltage guard-band for temperature, process and aging variations.

The growing limitations of analog LDOs to meet low voltage operation, fast response times and automated integration with digital load circuits point to the need of designing newer types of LDOs. These designs should not only power digital load circuits optimally right at the PoL but must also adapt under changing load requirements. This research contributes towards achieving these goals by building digital and digitally-assisted hybrid LDOs as summarized in the next subsection.

1.3 Contributions of this Thesis and Chapter Outline

To improve state-of-the-art and overcome the newer challenges posed by transistor and voltage scaling and heterogeneity of load, this dissertation research proposes digital and digitally-assisted hybrid LDOs. Digital LDO is especially suited for optimal power delivery for wide-range digital load circuits and digitally-assisted hybrid LDO powers all types of load circuits including digital and analog circuits.

Basic forms of digital LDOs were proposed [18, 19] before the beginning of this thesis

research as digital versions of an analog LDO. They supplement their analog counterparts in powering digital load circuits. Their compactness, ease of design, process and voltage scalability and the opportunity to embed them deep within a digital functional unit make them suitable for PoL voltage regulation. A literature survey of existing analog, near-digital and digital LDO topologies is carried out in chapter 2. The focus of this literature survey is to provide the reader with a holistic overview on the progress of on-chip linear voltage regulation. This section not only covers the designs published prior to the beginning of this thesis research but also includes contemporary and recent digital LDO designs which were built using the design concepts published in this dissertation research.

In chapter 3, the baseline structure of a digital LDO is explained. As the first major contribution of this thesis research, theoretical transient and steady-state modeling of a digital LDO is carried out in chapter 3 and 4. To the author's best knowledge, this is the first model which explains digital LDO operation in transient and steady-state. It shows that adaptive control is necessary in digital LDOs to ensure stability and wide dynamic range. The insights obtained from the model are verified using a discrete-component based digital LDO built on a printed circuit board and a test-chip built in 130nm CMOS process. The digital LDO in 130nm CMOS process uses adaptive control to maintain performance across a wide range of load current, supports operation down to near-threshold voltage and showed state-of-the-art performance in digital LDOs at the time of its publication [20, 21, 22].

Digital LDOs suffer from low PSR given the way their power stage is built using transistors as switches. Theoretical modeling of PSR in a digital LDO and control knobs to improve it are identified in chapter 5. This research is targeted towards making digital LDOs suitable for analog load circuits which demand a high PSR. A proactive supply noise rejecting digital LDO is built in 130nm CMOS process. It uses early warning signals from noisy voltage domains to temporarily improve the noise rejection capability of a digital LDO while satisfying a limited power budget [12].

In chapter 6, the dynamic range of a digital LDO is extended to power up a large digital core consuming in excess of 100mA of load current. This design also decouples the transient and steady-state performance of a digital LDO by using asynchronous non-linear gain control. It allows fast transient performance against large load current steps expected in a big digital load circuit like a microprocessor core. A test-chip is built in 65nm CMOS to experimentally verify the performance of the design. It shows the highest operational voltage range (0.15-1.2V) and static peak current efficiency (99.9%) in digital LDOs to-date. All this is achieved while ensuring a fast transient performance.

To overcome the intrinsic limitations of digital LDOs like steady-state voltage ripple and supply noise rejection capacity and achieve voltage regulation for all type of load circuits, digitally-assisted hybrid LDO using switched mode control (SMC), designed in 130nm CMOS process, is covered in chapter 7 and 8. This topology is the first hybrid LDO that uses an analog and a digital LDO in parallel and divides their activity based on a voltage error signal. This design inherits the steady-state performance and small signal accuracy of an analog LDO and the transient performance of a digital LDO [23] with a minimum increase in design complexity. Theoretical stability modeling of the hybrid LDO using SMC is also provided in chapter 8.

Building further on this hybrid LDO structure, SMC is employed to design a flexible LDO macro enabling a reconfigurable PSR design for wire-line I/O applications in chapter 9. The design is built in a 130nm CMOS test-chip and shows a wide range of energy-efficiency trade-off with PSR. Finally, insights drawn from these new LDO topologies are summarized and some comments are shared with the reader on future of on-chip voltage regulation research before the thesis is concluded.

CHAPTER 2
LITERATURE SURVEY

This section covers the use of LDOs in on-chip power management. We first briefly cover analog LDOs and their use in on-chip power management. It is followed by a detailed chronological description of design and development of hybrid, near digital and all-digital LDOs for on-chip power management.

Analog LDOs have been used in standalone and in cascade with switching regulators to supply power to portable electronics [15, 24]. Work on standalone ICs containing LDOs can be traced back to early 90s for generation of sub-5V voltage levels from the battery [25]. Besten et al., showed embedded down-conversion and regulation from 5V down to 3.3V in 0.5μm CMOS process for digital load ICs [26]. It was a high current delivery design capable of providing up to 300mA of load transients at a cost of 750μA quiescent current. The design had an NMOS based power transistor controlled through a charge pump based replica circuit. Since the transconductance of the PMOS device was less (true in older technologies) than that of an NMOS, IBM also showed a similar gate-boosted NMOS LDO to down-convert system supply voltage from 3.3V to 2.5V in 0.25μm CMOS process [27].

First instances of fully integrated low-voltage LDO designs for on chip applications made headway in late 1990s. Work by Rincon-Mora [15] showed near 900mV regulation from a 1V supply delivering 18mA at the cost of 23μA quiescent current. The design was implemented in 2μm CMOS process with an added p-base layer. It used a transient boost circuit between the error amplifier and PMOS based power device to enhance performance against voltage droops due to sudden changes in load current but used a large off-chip capacitor to stabilize the system. On-chip power management efforts before that were more application specific like for DRAM [28] and SRAM [29] and failed to meet the

requirements of general purpose LDOs.

Subsequent designs [15, 14, 16, 17] predominantly used PMOS as power device in LDOs. It allowed low dropout voltage operation as opposed to the NMOS based LDOs for on-chip applications. This basic configuration of an LDO with an error amplifier controlling a big PMOS power device required the use of an on-chip capacitor in Miller configuration to ensure stability. It improved the overall stability of the system but at the cost of reduced bandwidth and transient performance. This prompted a wave of research in innovative on-chip circuit topologies specifically targeting the large dynamic range of load circuits without the use of bulky off-chip capacitance. Leung, Mok [30] showed a damping factor controlled LDO capable of recovering from large voltage droops due to 100mA load step in 2μs. The design was based on three-stage amplifier and eliminates the bulky off-chip capacitor required for stability. Intel [14] presented a dual-loop topology in 90nm CMOS, decoupling reference tracking from transient performance using a replica based LDO design. The inner loop supplied the load current demand using fast flipped voltage follower stage [31]. The outer loop consisted of a two-stage op-amp and it controlled the inner loop using feedback from a smaller replica of the inner loop to track the reference voltage accurately. This design showed a full on-chip implementation with a capacitance budget of only 0.6nF for a load range of 100mA allowing less than 100mV of voltage droop. It achieved the best figure of merit for LDOs at the time of its publication but at a cost of very high quiescent current of 6mA. Milliken et al., [32] showed a fully on-chip LDO with a differentiator in the Miller capacitance feedback to allow fast transient recovery. The design used a small capacitance of 100pf at the output and a small quiescent current of 65μA. Since it was designed in 0.35μm CMOS, it could only regulate at a high voltage of 2.8V from a 3.5V supply voltage. Other frequency compensation techniques to keep stability and provide comparable performance have also been explored in [15, 14, 16, 17] targeting a narrow operating range. A fast LDO, suitable for on-chip application, proposed by Man et al., made use of two transistor flipped voltage follower configuration to allow

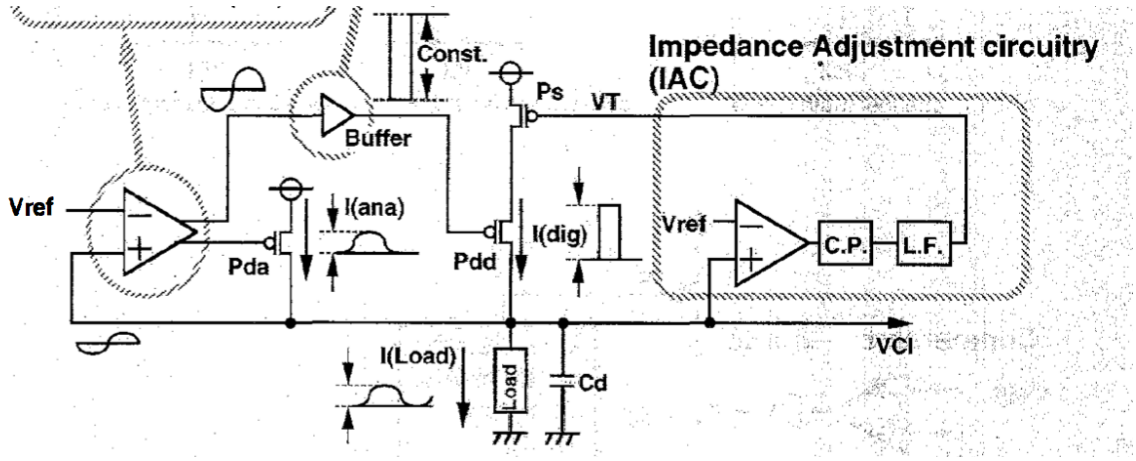


Figure 2.1: Analog LDO with digital-assist to improve transient performance powering DRAM.

fast transient response times [33]. It was particularly suited for low current and capacitance applications but faced scalability questions given its simple design. At lower supply voltages, operational range of analog LDOs is limited but it can still provide state-of-the-art performance in that limited range. Lu et al. [34] showed a PSR of -15dB at 1 GHz and 100ns response time for 10mA load steps at a regulated voltage of 1V from 1.15V supply. Similarly, Chen et al [35] showed a regulated voltage of 0.6V from a supply of 0.65-0.9V capable of providing up to 10mA load current in its highest dropout configuration.

To meet the wide operational range of digital load circuits that operate at various DVFS points, undergo large load transients, operate at very low voltages, and allow easy process integration and voltage scalability, all-digital LDOs have recently been the topic of profound interest. The first work in this direction can be traced back to Ooishi et al. in [36] as shown in fig. 2.1. It presented a hybrid LDO for fast transient performance at low quiescent current consumption powering DRAM. The design used a parallel combination of an analog LDO and a digitally controlled cascode transistor to meet fast transient load current requirement. The design incurred a large area overhead for output regulation voltage of 2.8V from a supply voltage of 3.5V. Another near digital LDO was published [37] in 2009 as shown in the fig. 2.2. As opposed to a digital LDO, where PMOS transistor are used to provide voltage regulation, this design implemented supply hopping i.e., allowed

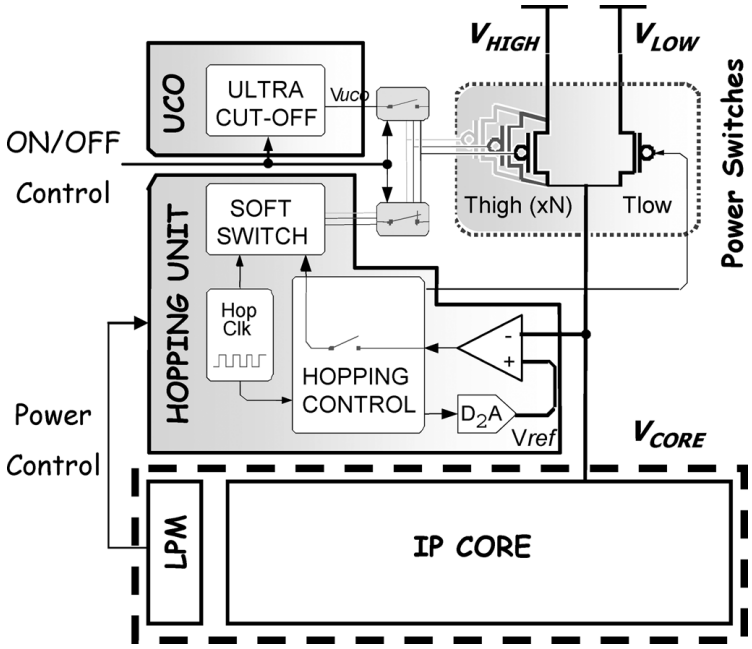


Figure 2.2: Voltage hopping based power delivery system.

fast switching between two supply voltages for two separate power modes. Although, this was not a regulator but the controller design preceded an equivalent digital LDO designed by Okuma et al., [18]. The work in [18] can be regarded as the first demonstration of an all-digital LDO capable of providing voltage regulation. The design was synchronous and used a master clock. It compared the regulated voltage with a reference voltage using a sense amplifier based comparator and made decision to turn on/off PMOS transistors in an array through a shift register based control logic. The digital LDO was developed in 65nm CMOS and the design schematic is shown in fig. 2.3. It achieved 0.45V regulated voltage from a 0.5V supply voltage with 98.7% current efficiency and 2.7μA quiescent current for 200μA load current. Although, the performance metrics were nowhere near the performance of an analog LDO but it, nevertheless, showed NTV operation. In a follow-up work, Hirairi et al. [38], combined a 16-bit integer unit with a digital LDO. The regulated supply voltage adapted itself through a digital LDO using parity based error prediction and detection. This work serves as a seminal work in the co-design of a digital LDO with digital load circuit as depicted in fig. 2.4. It showed 13% power saving by operating the system

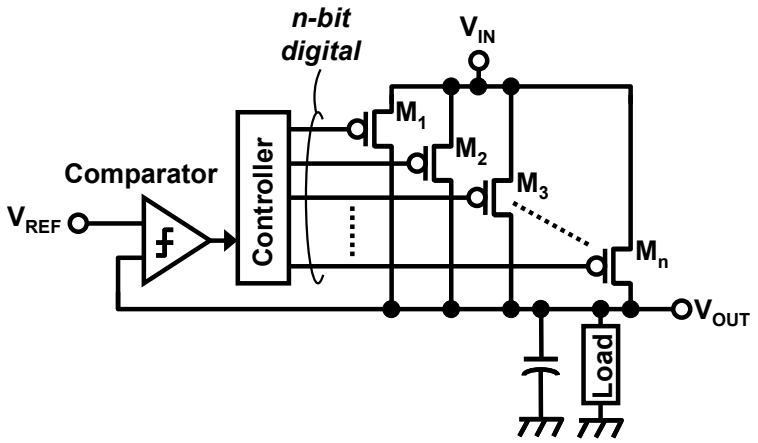


Figure 2.3: First implementation of a digital LDO by Okuma et al.

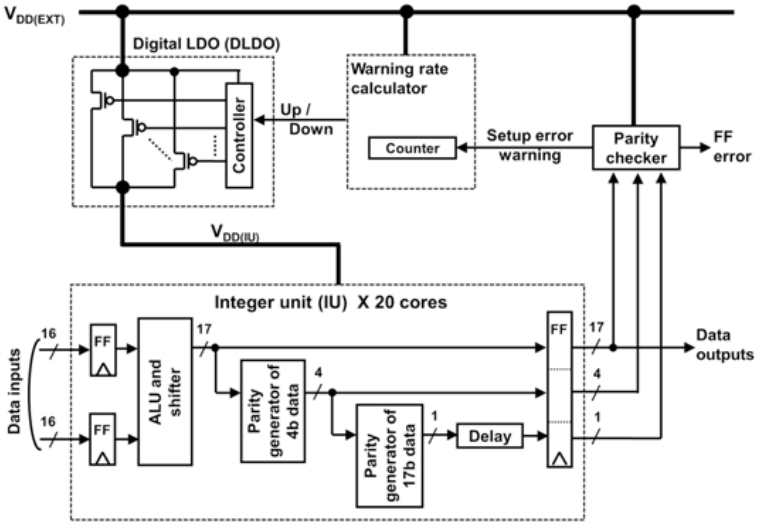


Figure 2.4: Digital LDO for minimum supply voltage delivery using parity based error prediction and detection.

near threshold voltage in 40nm CMOS process.

Given the discrete nature of clock based digital LDOs, providing small signal gain is not possible. Even if the digital LDO is used in high performance mode with a fast clock, the clock distribution network incurs a prohibitively large power overhead. To compensate for this limitation, continuous time digital LDOs were presented in [39, 40, 41]. The operation in [39] is based on a combinational logic called the bidirectional asynchronous wave pipeline (BAWP). BAWP can be considered as the clock-less equivalent of the shift register based PMOS transistor array control in a discrete-time digital LDO. Instead of generating

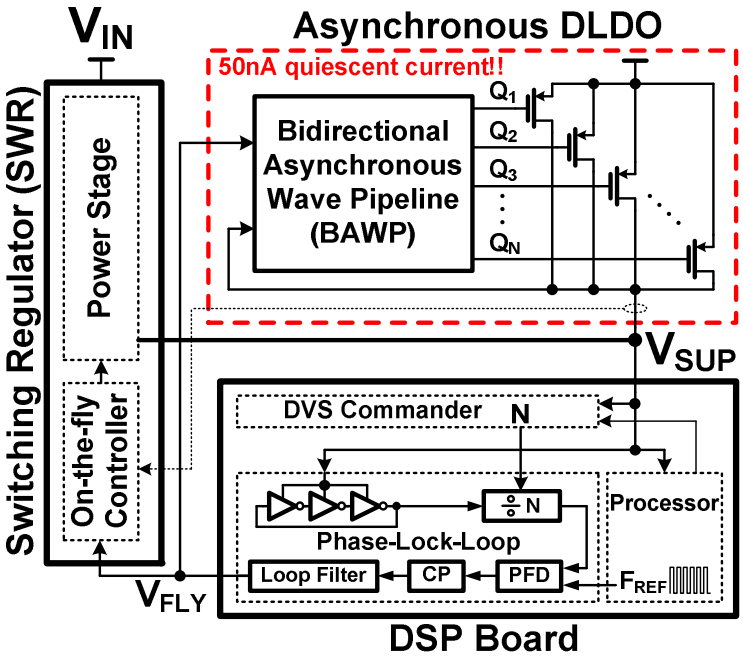


Figure 2.5: Continuous-time clock-less implementation of a digital LDO.

the direction signal based on a clock to increase or decrease regulated voltage, a combinational logic is used to propagate the direction signal asynchronously from one PMOS to another as shown in fig. 2.5. The design provided faster control then clock based designs due to lower latency but suffered from lack of adaptation under varying load current conditions and incurred a larger area overhead. Nevertheless, this digital LDO was used in parallel with a switching regulator and achieved a 150mV change in reference voltage in 40ns. It made this dual digital LDO and switching regulator topology suitable for fast voltage scaling. [40, 41] made use of the phase difference between the clocks generated by the reference and regulated voltages as can be seen in the design schematic of fig. 2.6. This topology achieved tight small signal regulation and low voltage operation down to 0.6V in 32nm CMOS. Since the design operated on phase difference, it was prone to performance variations due to switching noise, mismatches and delay between the clocks. IBM demonstrated use of a hybrid dual loop LDO topology to power a DDR3 I/O circuit [42], shown in fig. 2.7, and employed an equivalent design in power8 processor[10]. This design was based on a digitally calibrated outer loop which generated reference voltages [42]

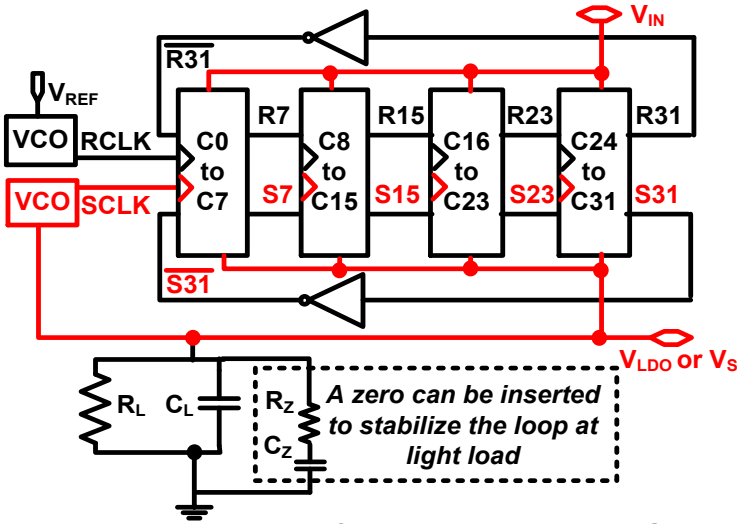


Figure 2.6: Phase difference based continuous-time digital LDO.

or digital codes [10] for distributed micro-regulators to achieve sub 10mV load regulation accuracy at low dropout voltage of less than 100mV. Each micro-regulator used a current mode charge pump based sense amplifier to turn on/off a PMOS transistor to regulate the output voltage. This micro-regulator can be interpreted as a continuous time bang-bang control based digital LDO. The design achieved high performance but suffered from a very low current efficiency of 77.5%. The more recent version employed in power8 processor showed improvement and a power efficiency of 90.5% [10].

2.1 Impact of this Thesis Research

The digital LDO built as a part of this research meets the requirements of digital load circuits and the hybrid LDO meets the requirements of both digital and analog load circuits [43, 23]. Following the literature survey chronologically, the digital LDO presented in chapter 3 was published at this time. This design captured the operational fundamentals of a digital LDO and has spawned further research after its publication. A brief description of these follow-up designs by both industry and academia is provided to help the reader get an updated perspective on the research in this direction.

Among the most notable recent publications is the digital LDO built in 22nm CMOS by

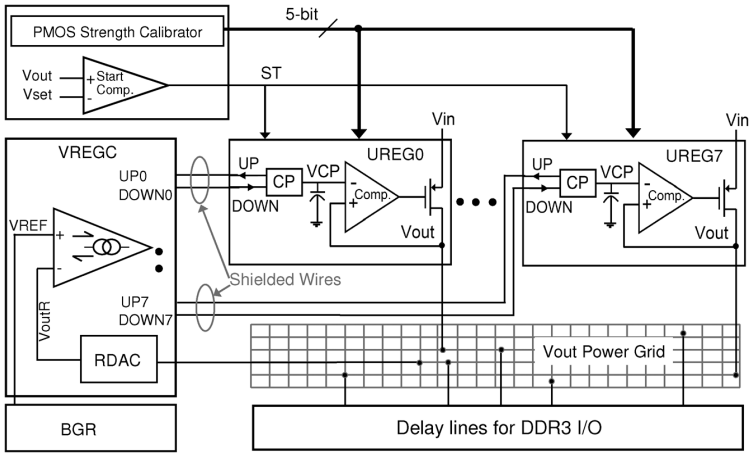


Figure 2.7: Dual-loop micro-regulators based LDO system for fine-grain power management.

Intel [11]. It builds on a similar design methodology as the digital LDO presented in chapter 3. It specifically utilizes a digital LDO to achieve low supply voltage and low dropout operation to extend the operational range of a switched capacitor based voltage converter. To further establish the relevance of the digital LDO, this design uses the power switches already in place to enable power gating of digital load circuits resulting in minimum area overhead.

Similarly, another recent design by Samsung [44] builds a dual-loop LDO utilizing control methodology like SMC (presented in chapter 8) paving the way for commercial deployment of digital LDOs in mobile applications. This design showed very good transient and steady-state performance but its voltage operational range is limited to only one operating point to guarantee uniform performance through the complete load current range. Yang et. al [45] used an asynchronous shift register based control stage and increased the load current range of the digital LDO by employing an array of output power transistors with multiple sizes. Although this increases the control latency due to the increased controller complexity but allows a good balance between transient performance and steady-state voltage accuracy.

Instead of using a global clock to synchronize the controller operation, [46] uses an

event based design using a level-crossing ADC to sample the output voltage continuously and control a quantized power stage. The design shows limited operational range in terms of load current given the lack of adaptation but provides a continuous-time implementation of a low supply voltage digital LDO. This event based detection saves clock power consumption but increases the design overhead to ensure that the level-crossing ADC dynamic range is larger than the expected voltage range.

Commercial processors incorporating similar digital LDO topology as presented in chapter 3 are available by the time this dissertation research concluded. Most notable among these designs are the high performance processor designs from AMD [13] and Oracle [3].

Complex controllers have also emerged over the last few years which incorporate multi-bit ADCs and multi-size power stage quantization to enable different trade-offs on LDO metrics. [47] uses a binary sized power stage to enable fast transient recovery and switches to continuous time control of a small power MOSFET to achieve small ripple during steady-state. The design performs well for small current ranges (a few mA) but suffers from large overshoot if the load current range is extended to a scale of tens of mA. This is because in case of a small load current step, the minimum action switches a large power MOSFET (binary sized) at the beginning of the control action creating a large mismatch between the load and source current. [48] uses a multi-sized, quantized power stage to achieve PID action and implements strength adaptation to reduce the limit cycle oscillations (first established in this thesis research) resulting in small ripple during the steady-state. This design shows a large operational range but requires multiple clock cycles to achieve complete settling.

Given the effectiveness of using a digital LDO for digital load circuits, several other designs can be found in the recent literature which follow similar design concepts for their specific application. A common denominator in these designs is the necessary requirement of controller adaptation with changing load conditions to enable a large operational range

of the digital LDO. This finding can be attributed as one of biggest research contribution of this thesis. The hybrid LDO topology has been recently published and its impact cannot be gauged at the time of publication of this dissertation.The author would like to mention that recently there has also been a trend to incorporate biased power stage inside the design of a digital LDO. Although this might be suitable for certain applications but these LDOs fail to fit the definition of a digital LDO and it is more appropriate to categorize them in analog LDO category.

CHAPTER 3

DIGITAL LDO WITH ADPATIVE CONTROL

Digital LDO in its most basic construction is a discretized version of a basic analog LDO as shown in chapter 1. The error amplifier in analog LDO is replaced with a clocked comparator which makes a digital binary decision of whether the regulated voltage (V_{REG}) is larger or smaller than a reference voltage (V_{REF}) and turns off or on, respectively, one of the power transistors in an array of power transistors to achieve regulation (V_{REG}=V_{REF}). This baseline digital LDO was first proposed by Okuma et al. [18].

Despite their potential advantages in providing fine-grained voltage regulation, the baseline digital LDOs suffer from slow transient response to large load current steps and suffers from degraded steady-state stability if transient response is improved. This trade-off is due to their synchronous and quantized construction. Furthermore, the sampling frequency of the digital LDO (as discussed in Section 2) controls its damping constant. Under a wide load range, the control loop can become power inefficient, heavily under-damped and even unstable. We address these two critical challenges, namely; transient performance and loop stability in this chapter and propose a digital LDO with adaptive control for ultra-wide dynamic range and temporary reduced stability for fast large-signal transient response.

The LDO macro fabricated in a 0.13μm LP CMOS technology features greater than 80% current efficiency across a 50x current range, and 8x improvement in transient performance (over the baseline design) in response to large load current steps which occur during wake up and clock gating/un-gating among other large power state transitions of digital circuits. The baseline design comprises of a barrel shifter that digitally controls 128 identical output PMOS transistors to provide regulation. To provide high efficiency with target stability under a large current range, we employ autonomous adaptation of the

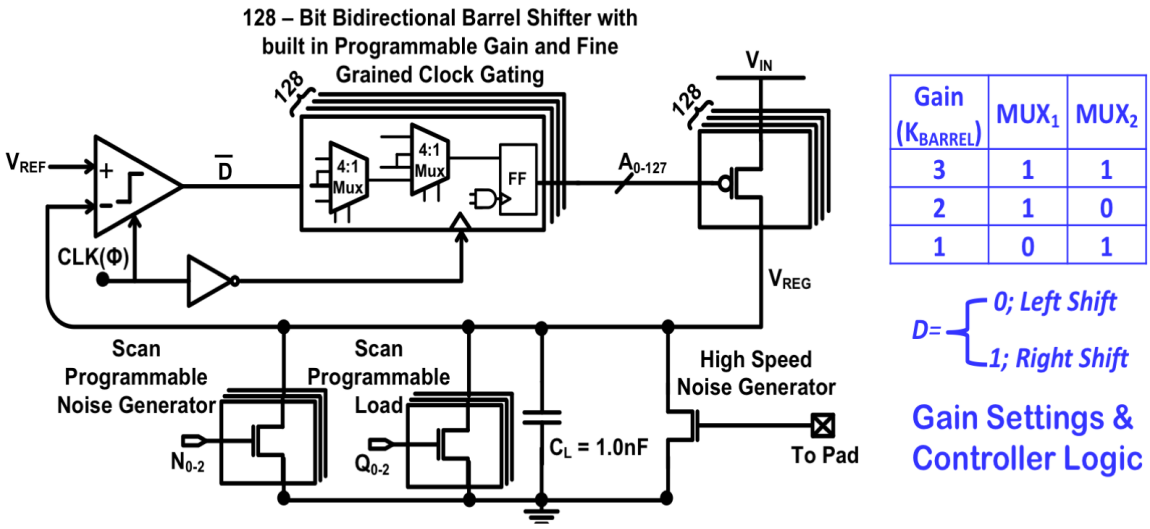


Figure 3.1: Fully-digital low-dropout (DLDO) regulator with digitally programmable loop gain and fine-grained clock gating.

clock frequency (F_S) with changes in the load current. Similarly, to overcome the reduced small-signal gain offered by the output PMOS array working in triode region, we introduce reduced dynamic stability as a design technique for fast transient response. The idea is to temporarily make the control loop marginally stable when a large load step occurs. It makes the system more agile and fast without compromising the run-time stability and enables high transient performance. The test-chip measurements corroborate the models as described later in this manuscript.

The outline of rest of the chapter is as following. In section 1, the baseline design of the LDO macro is described with its linear transient control model and steady-state behavior. In section 2, implementation of the autonomous adaptation circuit is elaborated. It is followed by an introduction to the concept of reduced dynamic stability (RDS) and its implementation in section 3. Section 4 presents measurement results from a prototype test-chip and a comparison with competing designs.

3.1 Baseline Design

The baseline design of the digital LDO is presented in fig. 3.1. The design consists of three major sections. The first section samples the output voltage and is implemented with a single-bit comparator. It is followed by a digital control section implemented through a barrel shifter. Finally, the output power MOSFET (PMOS) array provides load current and performs regulation [49]. A clocked sense-amplifier based comparator with an output latch [50] functions as a single-bit comparator. If output voltage (V_{REG}) is greater than V_{REF}, the comparator outputs a high (1) on the positive clock edge and a low (0) otherwise. As compared to a clock-less op-amp based comparator, this topology offers performance adaptation based on changing the clock frequency and reduces static power consumption. The output from the comparator gives the shift direction to a 128-bit bi-directional barrel shifter. This barrel shifter has a modular design to allow both externally programmable gain and fine grained clock gating. If V_{REG} is below V_{REF}, more PMOS transistors are turned on translating into a right shift operation. Otherwise, a left shift is performed to turn off PMOS transistors. The barrel shifter is scan programmable and provides a shift of 1,2, or 3 PMOS transistors in a single clock cycle. To reduce the propagation delay of the control signal, double clock edge triggering is employed. The comparator samples at the positive clock edge and the barrel shifter updates on the following negative clock edge. The magnitude of the shift in the barrel shifter serves as a gain control knob in the forward path of the LDO as we will explain later. The barrel shifter is implemented using two levels of signal multiplexing followed by a flip-flop. The first level of MUX allows a shift of 0, +2, -2 and the second level of MUX gives 0, +1, -1 to realize a complete shift range of -3, -2, -1, 0, 1, 2, 3. Here + and - define right and left shifts, respectively. Register programmable control signals MUX_1, MUX_2 are used to set the shift magnitude. This has been shown in fig. 3.2a.

Since the barrel shifter accounts for the largest digital part of the LDO and dominates

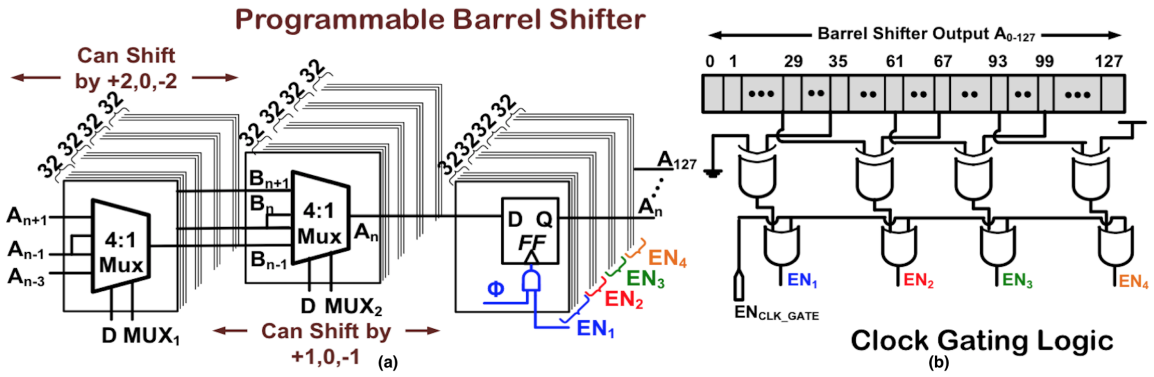


Figure 3.2: (a) Externally programmable 128 bit barrel shifter with 32 bit sections clock gating. (b) Sliding clock gating signal generation.

the overall clock load, a fine-grained clock gating is implemented to enhance power efficiency of the overall system. The 128-bit barrel shifter is divided into four 32-bit sections, which are clock gated in a sliding manner. Barrel shifter outputs are tapped from the boundary flip-flops of the 32-bit sections to generate enable signals for each 32-bit section, as shown in fig. 3.2b. For the maximum shift of 3, clock gating enables the next section as soon as ((Lx32)-3)th PMOS turns on for an increasing load current. Here L represents the enabled section and can be 1, 2, 3, 4. Similarly, for a decreasing load current, a lower section is enabled as soon as ((Lx32)+3)th PMOS turns off. This sliding logic keeps the relevant sections of the barrel shifter enabled while keeping the rest clock gated. In the worst case, a maximum of two sections are enabled if the load conditions demand that PMOS transistors at the boundary of these two sections are on.

The power output stage comprises of 128 PMOS transistors which are operated in triode mode thus realizing a fully digital LDO implementation. The PMOS are equally sized with a width of 400nm and a length of 120nm each. The array can provide a maximum current of 4.6mA for a dropout of 200mV with V_{IN}=1.0V. Scan programmable NMOS load transistors are implemented in the baseline design to achieve different values of steady state load current. To analyze the transient performance of the LDO, another set of scan programmable but externally triggered NMOS transistors are used for creating large, pro-

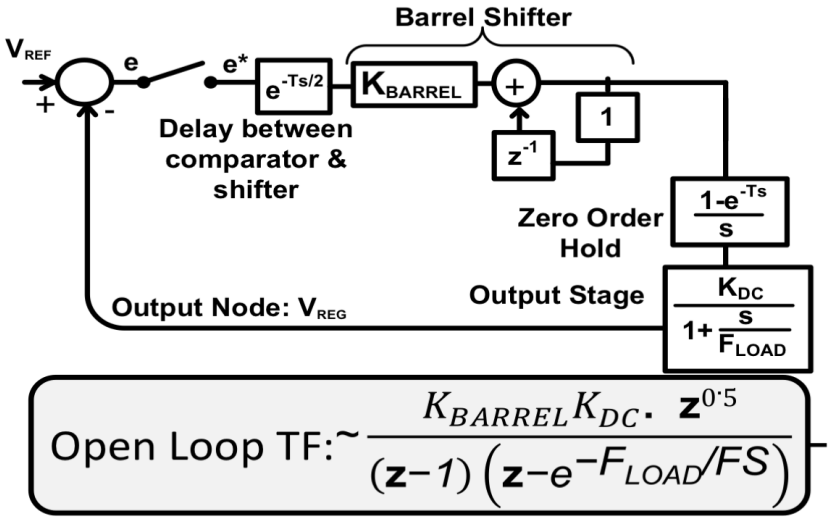


Figure 3.3: Second order discrete time transient model with open loop transfer function for the baseline design.

grammable and high-speed voltage droops. In the current design, a total capacitance of approximately ∼900pF is placed at the output node to mimic the capacitance offered by supply distribution grid (using metal routing) and a digital functional unit load [42]. In the next two subsections, we present both a linearized model for transient analysis and a non-linear model for steady-state analysis of the digital LDO. These models have been presented in detail in [49] and [21] and are reported here briefly for the sake of completion and understanding the trends in measured data. Experimental results in Section 4 demonstrate the validity of these models.

3.1.1 Transient Behavioral Model

The presented LDO design employs synchronous operation and as such its linear small signal model is represented in the z-domain to account for discrete-time digital control and operation. (see fig. 3.3).

The ADC or the single bit comparator acts as a voltage sampler and converts the con-

tinuous time error signal to its discrete time representation e*.

$$e^* = V_{REF}(nT) - V_{OUT}(nT) \tag{3.1}$$

The barrel shifter acts as a discrete time integrator and in its simplest implementation has $\alpha = 1$. The output of the shifter, which is a thermometer coded digital word (D(nT)) represents the number of pull-up PMOS that are on at a time instance, nT, where T is the period of the sampling ADC Clock. It can be written as

$$D(nT) = \alpha D((n-1)T) + K_{DIGITAL}e((n-1)T) \tag{3.2}$$

Here $K_{DIGITAL}$ is the overall gain of the digital control loop and is set by the programmable gain of the barrel shifter which controls its step-size. From Eq. 3.2 the transfer function D(z) is:

$$D(z) = K_{DIGITAL}e(z)/(z-\alpha) \tag{3.3}$$

The output of the shifter controls the number of PMOS that are turned on, and thus interfaces with a continuous time plant (power MOSFETs and the load). This can be modeled as a zero-order hold (ZOH) cascaded with a first-order plant whose output pole, a, is given by the load circuit. The s-domain model for ZOH followed by the plant is:

$$P(s) = (\frac{1-e^{-sT}}{s})(\frac{K_{DC}^{PLANT}}{1+\frac{s}{a}}) \tag{3.4}$$

Using Eq. 3.4, the corresponding P(z) in z-domain can be represented as

$$P(z) = \frac{K_{DC}^{PLANT}(1-e^{-aT})}{a}(\frac{1}{z-e^{-aT}}) \tag{3.5}$$

Thus, the open loop forward path transfer function of the digital LDO can be written in

z-domain as:

$$G(z) = \frac{K_{DIGITAL} K_{DC}^{PLANT} (1 - e^{-aT})}{a(z - \alpha)(z - e^{-aT})} \tag{3.6}$$

Here $T = 1/F_S$ is the time period of the sampling clock of the digital control. The plant load frequency (a) can be described as:

$$a = Z_{eq} || R_{pu} = \frac{Z_{eq} R_{pu}}{Z_{eq} + R_{pu}} \tag{3.7}$$

where $R_{pu} = (\frac{R_{on}}{D(nT)} + \frac{R_{off}}{N - D(nT)})$, $Z_{eq} = \frac{R_L}{1 + sCR_L}$ and N is the total number of pull-up PMOS transistors.

As can be observed in Eq. 3.6, the poles are located at $z = \alpha$ and $z = e^{-aT}$. Using unity feedback, the overall closed loop transfer function of the digital LDO in the z-domain is given as:

$$H(z) = \frac{G(z)}{1 + G(z)} \tag{3.8}$$

As evident from 3.6, one of the poles comes from the discrete integration at the unit circle boundary and the position of the other pole is given by both the load (F_{LOAD}=a) and the sampling (F_S) frequencies. A decreasing load current at iso-F_S, decreases F_{LOAD} which brings the poles closer together on the real axis. In z-domain this is equivalent to a decrease in the phase margin of the overall system. Therefore, the step response exhibits a higher overshoot and decreased damping resulting in an under-damped response. Similarly, an increase in the load current makes the whole system over-damped and shows greater stability but slower transient performance. This phenomenon is illustrated by the pole-zero plots and their equivalent load step responses (simulation criteria reported in the figure caption), as shown in fig. 3.4. On the other hand, increasing F_S enhances the transient performance of the whole system but equivalently, the system becomes under-damped. For extremely light load conditions, the system can become highly under-damped and eventually unstable. This motivates us to use an adaptive F_S, which can track F_{LOAD} during run-time such that the ratio (F_{LOAD}/F_S) is bounded and a target stability margin can be achieved across

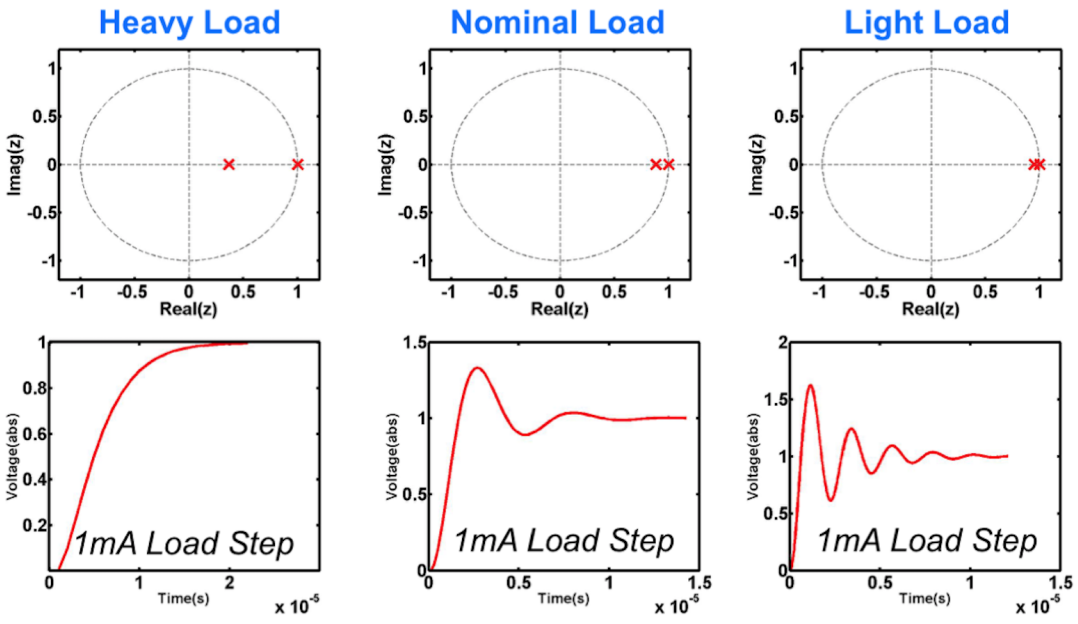


Figure 3.4: Simulations showing a decrease in phase margin for a 1mA load step with a constant F_S=50MHz for three different initial load conditions. I(Heavy)=5mA, I(Nominal)=1mA, I(Light)=100μA.

a wide dynamic range of load current conditions. The design details will be discussed in section 2. By similar arguments, a faster rise time and recovery from voltage droops of the output voltage can be achieved with an increased K_{BARREL} as illustrated from simulation results in fig. 3.5.

It should be mentioned here that the exact value of K_{DC}^{PLANT} is a function of load current, load capacitance and the power stage transconductance. All these parameters are subject to change under a load transient event. Therefore, identification of exact value of K_{DC}^{PLANT} to establish stability bounds can only be inferred using SPICE simulations.

3.1.2 Steady State Dynamics

The transient behavior model helps in understanding the LDO response to step changes in V_{REF} and I_{LOAD}. This linear model is inadequate in understanding the steady state behavior of a digital LDO which exhibits limit cycle oscillations. A detailed model is derived and analyzed in chapter 4 both theoretically and experimentally. The major insights from that

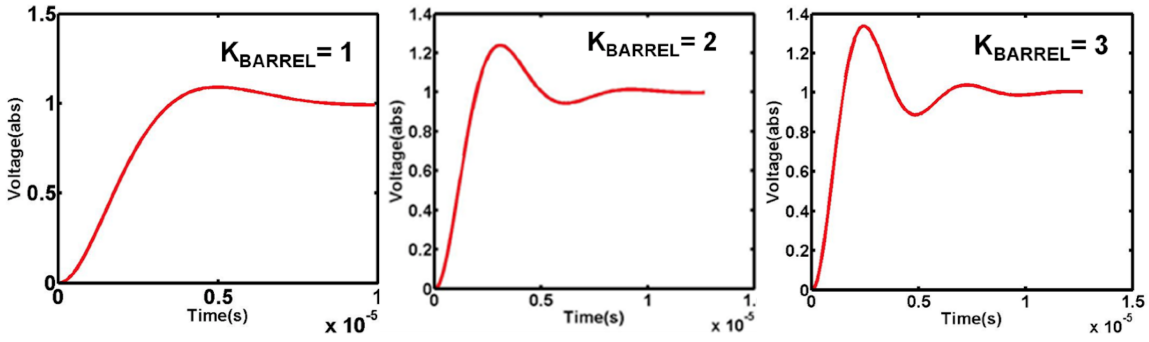


Figure 3.5: A faster rise but increased overshoot is observed in simulations with increasing K_{BARREL}. Here the initial load is 1mA and F_S=20MHz.

model are summarized here.

For a constant I_{LOAD} and F_S, a voltage ripple is observed at the regulated output voltage. Since, the PMOS transistors are operated as switches at a constant clock frequency, a number of these PMOS transistors turn on and off periodically in steady-state. The number of PMOS transistors turning on and off periodically is referred to as the mode of oscillation (n). The Nyquist criterion is then applied to develop necessary conditions on the existence of different modes of limit cycle oscillation. Interested readers are pointed to [21] or chapter 4 for more details on the model, and the key implications will be discussed here.

As the sampling frequency, F_S, increases (for iso-F_{LOAD}) the mode of oscillation increases. One of the consequences of an increased mode of limit cycle oscillation is a potential increase in the output ripple. However, the ripple is not a direct function of n. As long as the mode of oscillation remains unchanged a larger value of F_S/F_{LOAD} tends to decrease the ripple due to the filtering action of the output pole. However, with increasing F_S/F_{LOAD}, the mode of oscillation itself increases discretely. This leads to discrete jumps in the ripple voltage as described in [21] and will be discussed in Section 4. A theoretical analysis on existence and bounds of limit cycle oscillations in discrete-time digital LDOs with experimental verification is detailed in chapter 4.

3.1.3 Model Analysis

Based on the behavioral models for both transient and steady state performance of the digital LDO, the following challenges of a baseline design can be ascertained. 1) Although a high F_S results in faster transient response but it renders the system under-damped. It exhibits loss of phase margin and results in large overshoot of the regulated voltage with slow settling. This leads us to the notion of keeping F_S/F_{LOAD} bounded for a more consistent transient response across a wide dynamic range of operation. 2) A high F_S/F_{LOAD} is responsible for a higher mode of limit cycle oscillation. However, as F_S/F_{LOAD} increases, the filtering action of the output pole tends to reduce the overall ripple. Conversely, at low F_S/F_{LOAD} the output ripple due to the limit cycle becomes prominent. Both of these factors dictate that F_S with respect to a given output pole (F_{LOAD}) needs to be bounded. This motivates the need for adaptation to enable wide dynamic range of operation. Simulations reveal that an F_S/F_{LOAD} ratio of 5 to 10 provides an optimal trade-off between response time and over-shoot/phase-margin under constant load conditions [22].

3.2 Adaptation of Sampling Frequency with Changes in the Quiescent Point

In the current design, we perform an autonomous adaptation of F_S to ensure a consistent damping while maintaining a small ripple during steady state across the complete load range. As the load current is detected, it is used to select one of the three sampling clock frequencies F_{HIGH}, F_{NOM}, F_{LOW} once a steady state is established. These frequencies are generated through two current starved voltage controlled ring oscillators. VCO_1 provides F_{LOW} and F_{NOM} through its long and small chains, respectively, whereas VCO_2 provides F_{HIGH} and $F_{TRANSIENT}$. $F_{TRANSIENT}$ is used for large load transient events as explained later in section 3. These VCOs provide tight frequency control with small power consumption and require no level shifting. The control voltages are accessible to the pads that allow us to calibrate F_S. The 128-bit output PMOS array is divided into three regions representing

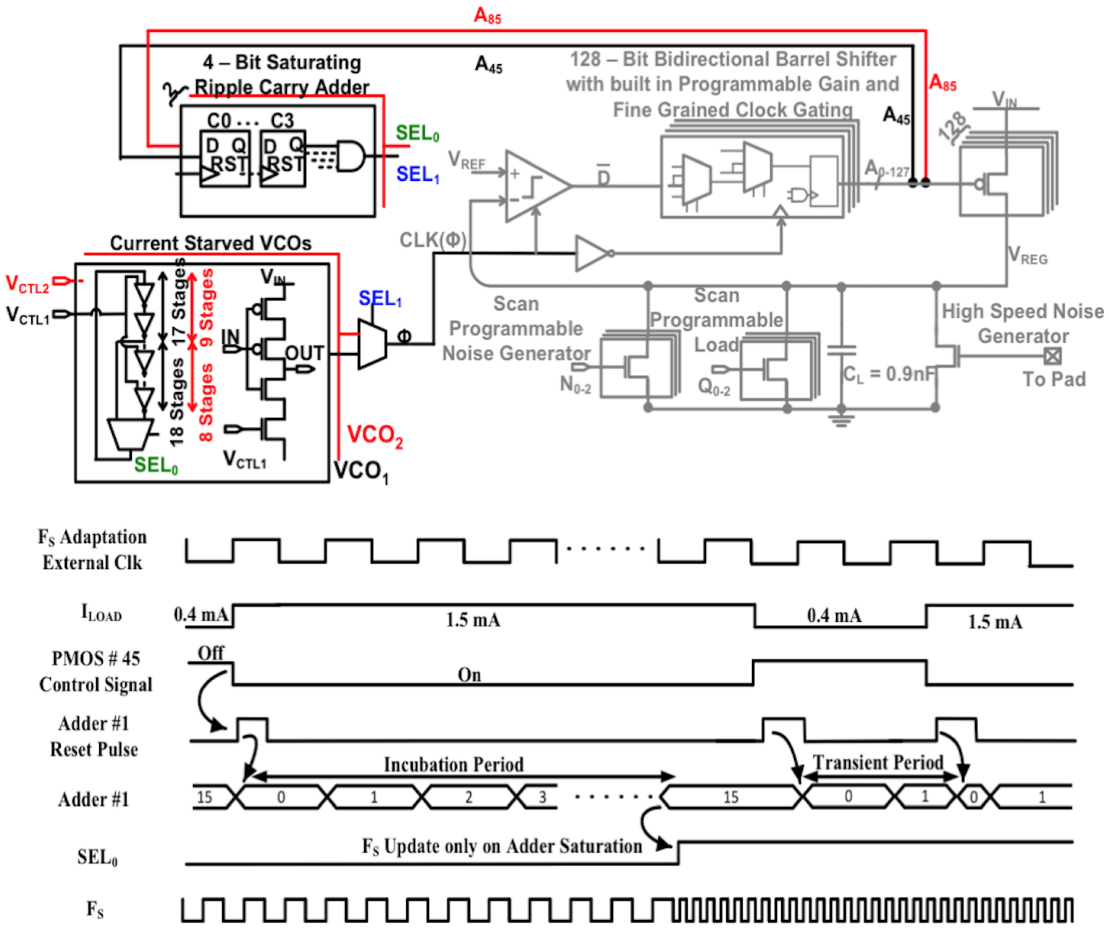


Figure 3.6: Autonomous adaptation of sampling frequency (F_S) across a wide dynamic range using current starved VCOs with steady state I_{LOAD} detection and corresponding F_S adaptation timing diagram.

I_{LIGHT}, I_{NOM} and I_{HEAVY} load conditions. I_{LIGHT} is classified until PMOS-45 turns on. I_{NOM} extends to PMOS-85 from PMOS-45 and I_{HEAVY} starts from PMOS-85. The steady state I_{LOAD} detector takes the control signals from bit-45 and 85 of the barrel shifter. A change on any one of these control signals indicates a change of steady state load region and creates a reset pulse for a 4-bit ripple carry adder. This adder is running from an external clock running at 5MHz controlled through an I/O pad. The time of a 4-bit ripple carry adder to saturation serves as an incubation period for steady state establishment whereas; a reset pulse before the adder saturates indicates a transient event. Once saturated, the adder stops and an appropriate F_S is selected to maintain a bounded F_S/F_{LOAD}. The F_S adaptation design

is added to the baseline as illustrated in fig. 3.6 with a representative timing diagram. The inclusion of incubation period through the adder decouples the fast regulation loop from the slow F_S adaptation to keep the system stable. The classification of the load current into high, nominal and low is based on a linear division of the total load range. It doesnt require any additional current detection hardware. Without loss of generality, other non-linear divisions are also possible.

3.3 Reduced Dynamic Stability (RDS) based Fast Transient Control

A lower F_S saves controller power and maintains small signal stability. However, digital load circuits undergo very large and infrequent load transients (during power/clock gating/un-gating). To address the limited run-time gain of the digital LDO, we introduce reduced dynamic stability (RDS) as a solution to improve large signal transient response. RDS is based on the notion of switched mode control, where the control loop can discretely switch from a stable, damped behavior to a quasi-stable behavior when the error voltage crosses a predetermined threshold (Δ). The main objective of RDS is to create a system response which combines faster rise time of an under-damped behavior and non-oscillatory settling of an over-damped behavior. To the authors knowledge this is the first application of switched mode control in PoL linear regulation. Thus, for large voltage droops, the system switches to a fast F_S (under-damped) at a threshold (V_{REF}-Δ_-) and comes back to slow F_S (over-damped) once V_{REG} is within some threshold (Δ) of V_{REF} as conceptually illustrated by fig. 3.7.

A digital LDO allows a seamless implementation of RDS with minimal overhead of circuit complexity. Fast droop and overshoot detectors based on sense-amplifier based clocked comparators are placed in parallel with the basic comparator of the baseline design as shown in fig. 3.8. V_{REG} is compared against a threshold (Δ) above and below V_{REF} and identifies an overshoot or droop. As soon as V_{REG} falls below V_{REF}-Δ, the droop detector selects a very fast sampling clock ($F_{TRANSIENT}$) available from VCO_2 ensuring a fast recov-

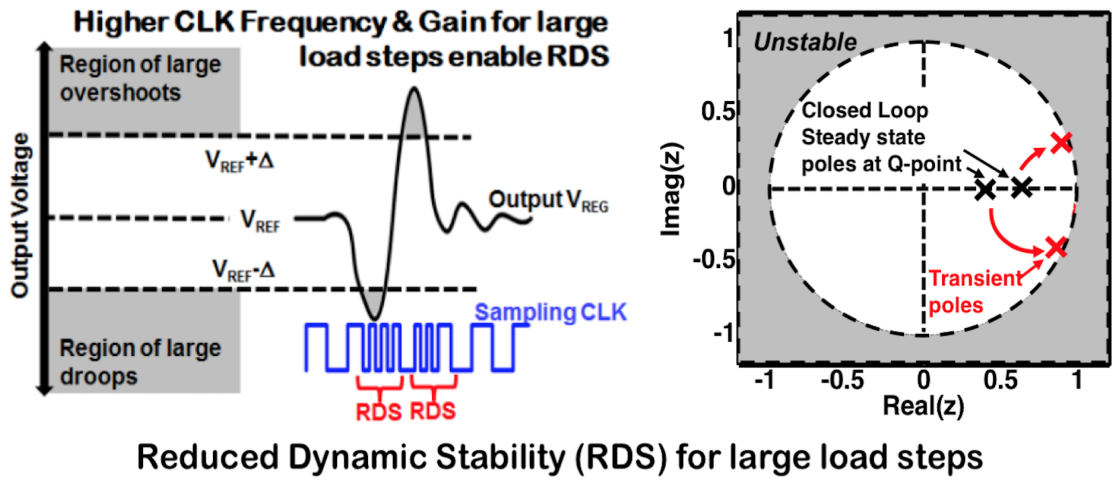


Figure 3.7: Conceptual representation of temporary stability trade-off for enhanced transient performance using RDS.

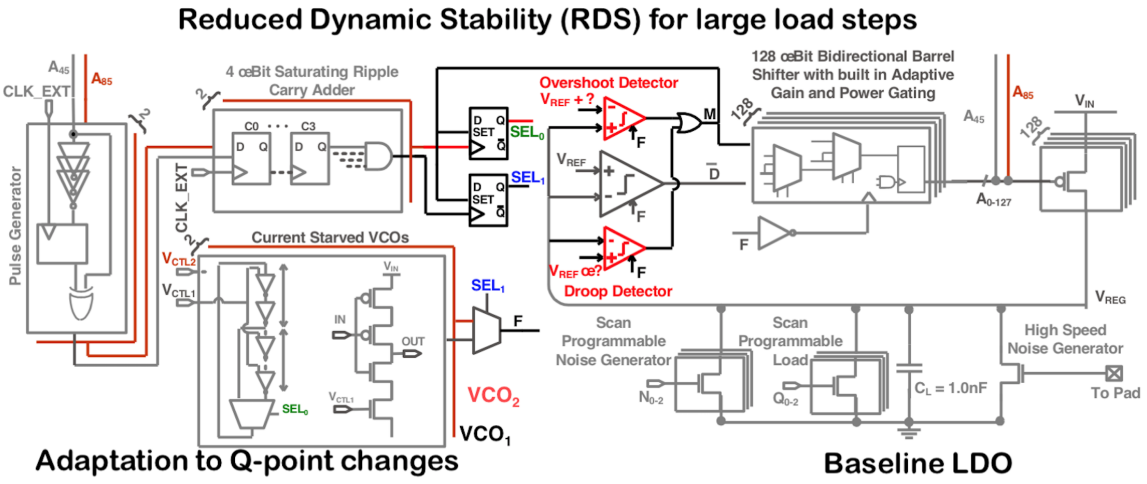
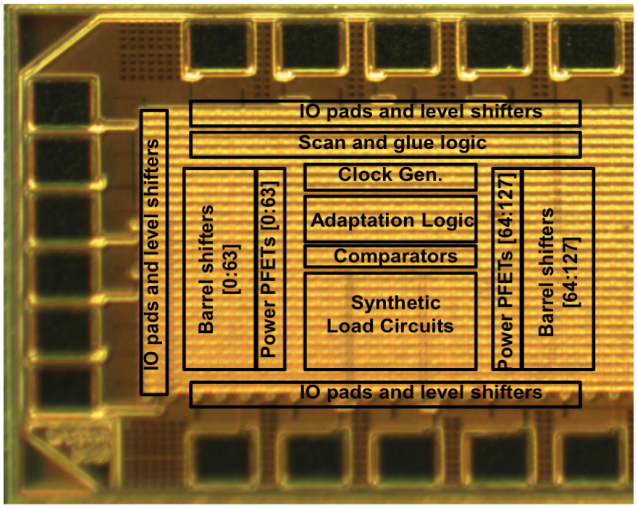


Figure 3.8: Droop and overshoot detectors detect large load transients. In response, a faster sampling clock and higher loop gain are enabled for faster recovery from droops and overshoots.



Process	IBM 130nm CMOS 8-M
Total Area	2 mm^2
Active Area	0.3552 mm^2
LDO Area	0.114 mm^2
Testing Interface	QFN Package

Figure 3.9: Chip micrograph, process and design specifications. The micrograph shows 1mm x 1mm which consists of the LDO and it shares the total $2mm^2$ area with another experiment.

ery. As soon as V_{REG} reaches back to V_{REF}-Δ, previously running steady state F_S clock is restored allowing a non-oscillatory return to the desired V_{REG}. Similarly, an overshoot is defined at a Δ above V_{REG}. In case of an overshoot due to a large load current decrease, $F_{TRANSIENT}$ is enabled to ensure a fast return to the desired V_{REF}. A smooth monotonic return of the V_{REG} to V_{REF} is ensured by enabling the damped steady-state response of the LDO. This is done by switching over to the previously running steady state F_S clock once the V_{REG} reaches V_{REF}+Δ. Both upper and lower threshold voltages as well as the target reference voltage are externally available on the pads. This allows us to calibrate the threshold voltage (Δ) for different drop-out voltages.

3.4 Test-chip Measurement Results

The digital LDO is designed and fabricated in IBM 0.13 μm 8-M LP CMOS (process V_{TH}≈420mV at V_{DS}≈500mV) process. It occupies an active area of 0.355 mm^2 with both load capacitance and test load as shown in the chip micrograph of fig. 3.9. The LDO is

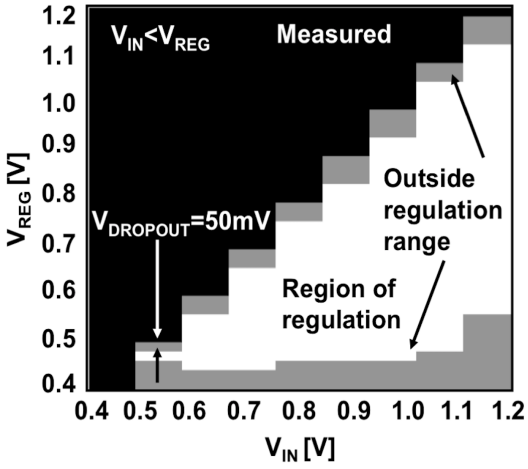


Figure 3.10: Measured shmoo plot representing regulation range of the designed LDO. Transistor V_{TH} is measured at 420mV at V_{DS} = 500mV. The white region shows regulation, the grey region shows the region where regulation could not be obtained and the black region shows an inoperable region where $V_{IN}<V_{REG}$.

capable of regulating the output voltage from 1.1 to 0.45 V from a V_{IN} of 1.2 to 0.5 V with a minimum dropout of 50 mV as illustrated in the Shmoo plot of fig. 3.10. The measured process V_{TH} is $\sim$420mV (at V_{DS}=500mV) and thus we can obtain regulation down to the near-threshold-voltage (NTV) region (V_{REG}=1.07x of process V_{TH}). The LDO is measured to provide I_{LOAD} from 4.6mA (maximum) down to 0.1μA (minimum). Both externally controlled and scan programmable NMOS transistors are implemented as load. They are used to generate both fast transient step currents and quiescent currents for complete characterization of slow adaptation and RDS across a wide dynamic range of load current. Fig. 3.11 illustrates the measured VCO frequency for the three steady state VCO loops (high, nominal and low) as a function of the control voltage (V_{CONT}). As adaptive selection of F_S is employed, a representative oscilloscope capture (fig. 3.12) shows the autonomous change of F_S after an incubation time. Selection of F_S should ensure a target settling time for small load transients that happen during workloads on digital circuits in steady state operation. Settling time (T_S) of load conditions from I_{LIGHT}, I_{NOM} and I_{HEAVY} monotonically decreases for increasing F_S as the measurement results show in fig. 3.13a. For a target settling time,

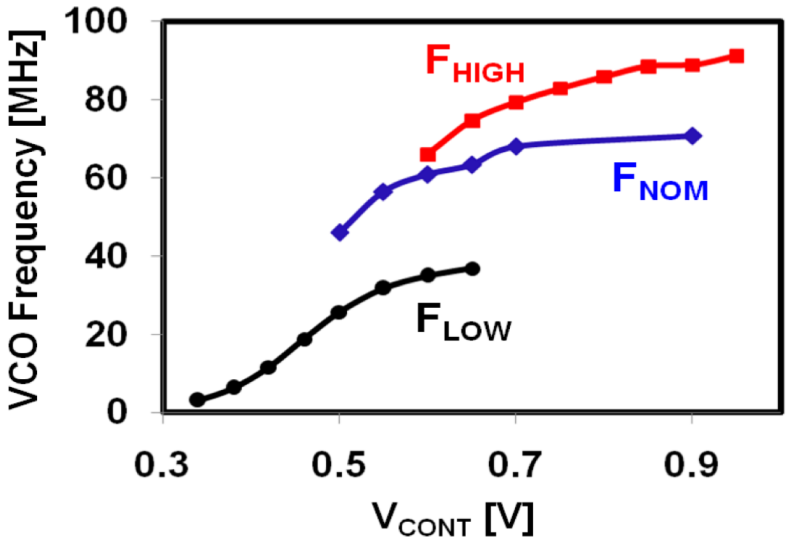


Figure 3.11: Measured VCO frequency with varying V_{CONT}. V_{CONT} is controlled and calibrated from an external pad.

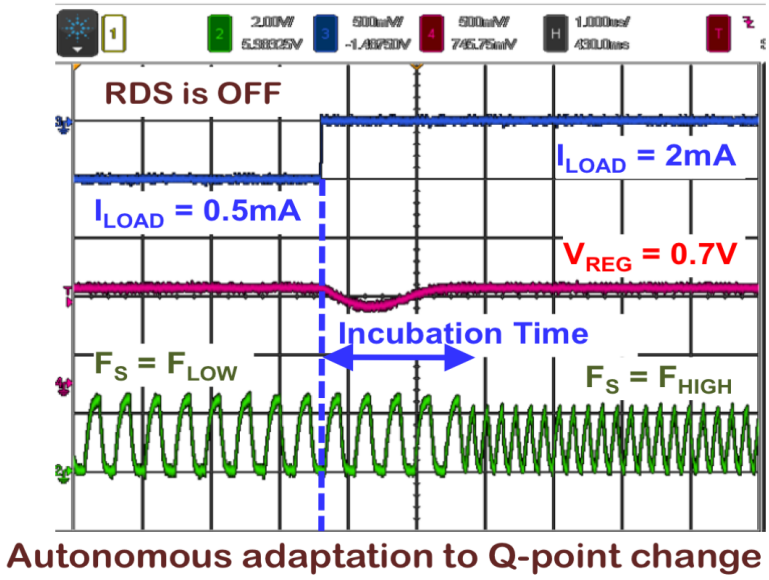


Figure 3.12: Representative oscilloscope capture illustrating adaptation of F_S with change in the quiescent current.

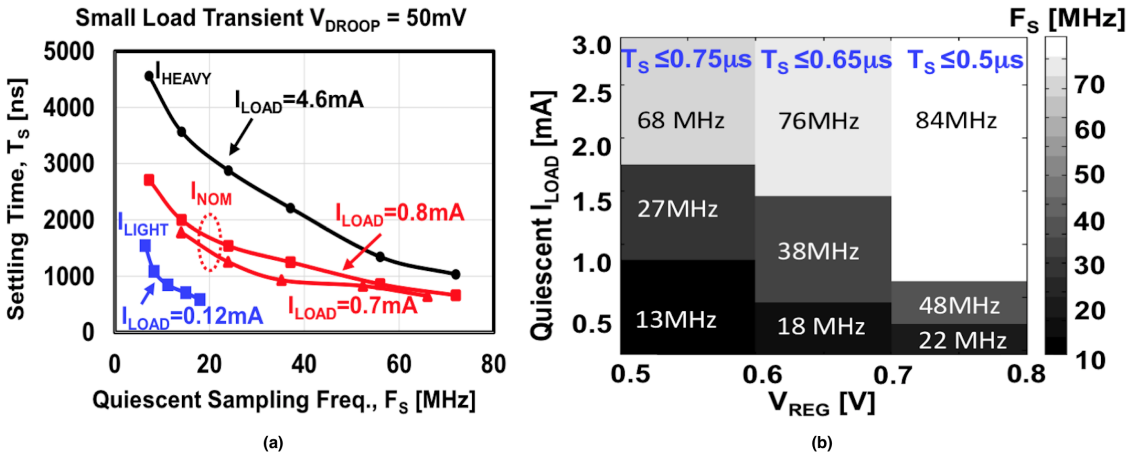


Figure 3.13: (a) Measured settling time (T_S) for small voltage droops vs increasing F_S for multiple I_{LOAD} conditions. (b) Frequency selection plot for iso-settling time performance for I_{LOAD} up to 3 mA using measurements. The different frequencies (as shown in the graph) are selected via calibration of on-die VCOs whose control terminal is exposed to the pads.

an adaptive F_S ensures consistent performance across the load current range. From fig. 3.13a we note that for light load conditions, I_{LIGHT} meets an iso-settling time constraint (of 1μs) with a smaller F_S as compared to I_{NOM} and I_{HEAVY}. With increasing V_{REG}, a faster transient response is often desired. We calibrated V_{CONT} for three different settling time constraints 0.75μs, 0.65μs, 0.5μs for V_{REG} between 0.5V and 0.8V and the corresponding frequencies are shown in fig. 3.13b. These represent current loads that create voltage droops of 50mV.

Large voltage droops associated with power state transitions shows a slow recovery in the baseline design motivating the use of RDS. A representative measured scope capture is shown in fig. 3.14 which shows switching to and from $F_{TRANSIENT}$ resulting in a faster settling as well as reduced droop and overshoot compared to the baseline case (Δ=50mV). During execution of a workload, the voltage transients on V_{REG} is expected to be less than 50mV and this sets the boundary between steady-state regulation and large signal transients [11]. Measured settling time for droops >50mV (in response to large current transients) is shown in fig. 3.15. The settling time in the baseline design shows a concave behavior as

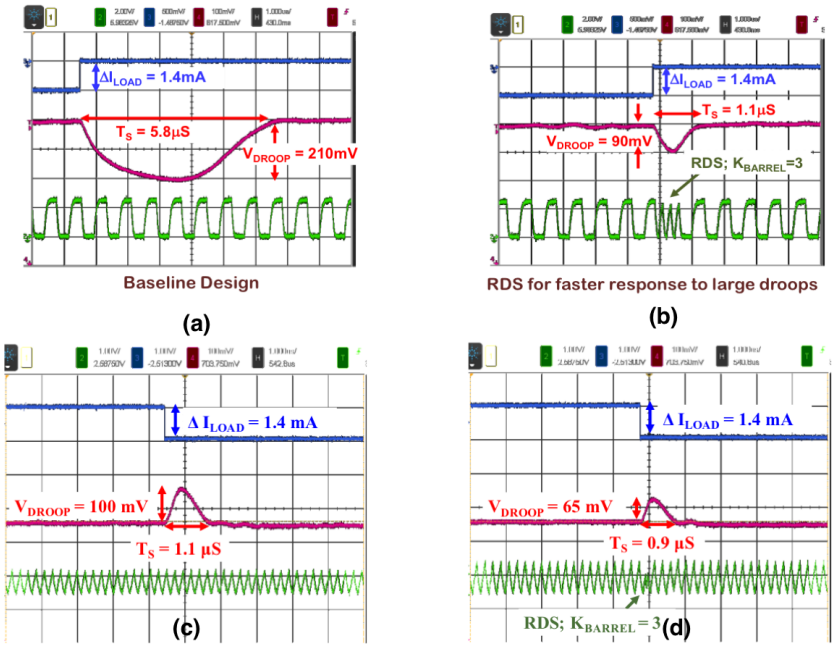


Figure 3.14: Representative oscilloscope capture demonstrating RDS when a large voltage overshoot (droop) occurs in response to a large load step down (up) in (a) and (b) ((c) and (d)). In digital circuits these are infrequent events that occur during clock/power un-gating (gating).

seen in fig. 3.15a. Initially, increasing F_S decreases settling time as the system becomes critically damped but eventually becomes under-damped and exhibits large overshoot when F_S increases further. RDS helps reshape this concave settling behavior and reduce the settling time under large load steps (for a 2.1mA load step). Along with switching to the transient frequency ($F_{TRANSIENT}$~400MHz), the barrel shifter gain is also set to its highest scan programmable shift value (=3) to provide a high loop gain. Compared to the baseline design an 8x improvement in the settling time is measured. The greater agility achieved during the under-damped region of operation also helps in decreasing the overall voltage droop (for iso-load-step). A worst case of 36% and a best case of 60% reduction in droop is measured when RDS is used as compared to the baseline design (fig. 3.15b). Fig. 3.16 illustrates the measured settling-time with increasing $F_{TRANSIENT}$ and constant F_S of 24MHz. We note that the settling-time first decreases as $F_{TRANSIENT}$ increases. However, as $F_{TRANSIENT}$ increases beyond an optimal value, the composite system becomes under-damped and goes

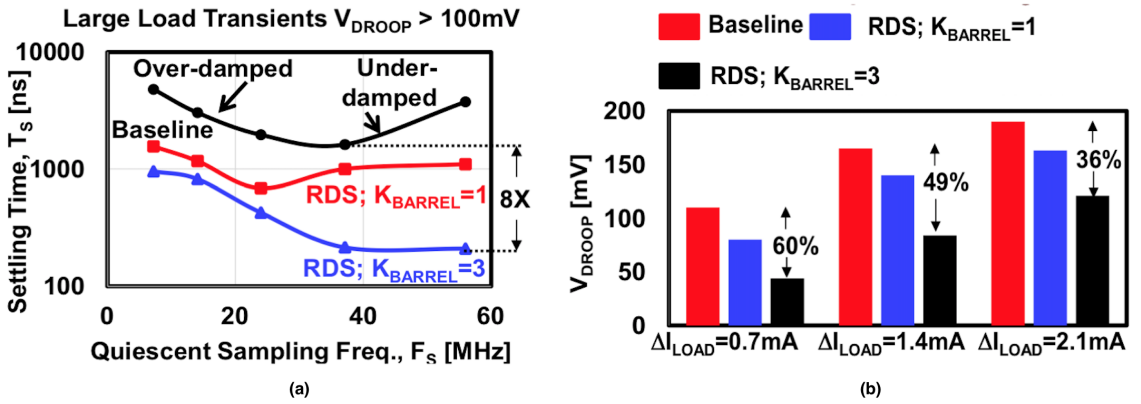


Figure 3.15: Measured settling time, T_S (for small droops) with adaptation for autonomous choice of F_S. (a) RDS allows 8x improvement in T_S for large load transients and (b) 36% to 60% reduction in V_{DROOP} when compared to the baseline design.

through larger and larger overshoots. This happens even when the sampling frequency is switched back once the output voltage reaches $V_{REF}\Delta$. This overshoot can be decreased by increasing Δ, which provides a trade-off between performance and the region of operation when RDS is activated. For Δ=50 mV and steady state F_S=24MHz, measurement results (fig. 3.16) show that $F_{TRANSIENT}$ over 424 MHz exhibits under-damped response.

Fine grained clock gating helps achieve large decrease in controller power. These power savings become higher as the operating frequency increases. Over 25% decrease in controller power is measured at a V_{IN} of 1V and over 50% is achieved for 0.75V at an F_S of 95MHz and 65MHz respectively, as shown in fig. 3.17. A 46x load current range from 0.1μA (with a single PMOS turned on) up to 4.6mA is measured which shows regulation across the entire dynamic range. This is shown in fig. 3.18 where the measured design regulates from 1.1V down to 0.5V with a minimum dropout of 50mV. A measured load regulation (fig. 3.18) of $<$10mV/mA is achieved. A worst case line regulation of 3.4% is measured on V_{REG}=0.55V for a V_{REG} of 0.55V to 1V with V_{IN} ranging from 0.64V to 1.2V as illustrated in fig. 3.19a. Similarly, a tight regulation of $<$5% (at worst-case) under a wide range of load switching frequency is measured as shown in fig. 3.19b. It should be noted that measurement of load and line regulation are limited by the voltage ripple at the

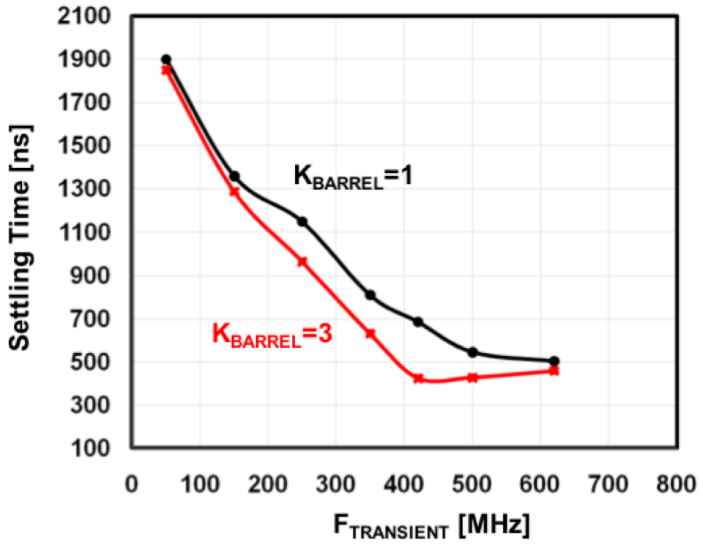


Figure 3.16: Measured settling time with varying $F_{TRANSIENT}$ for two different values of K_{BARREL}. Here the initial load current is 1mA, the lead step is 2mA and D=25mV. Optimal settling is achieved for an $F_{TRANSIENT}$~425MHz when steady state F_S=24MHz. We note that for high K_{BARREL} and $F_{TRANSIENT}$>425MHz, the total system becomes underdamped and the settling time starts increasing.

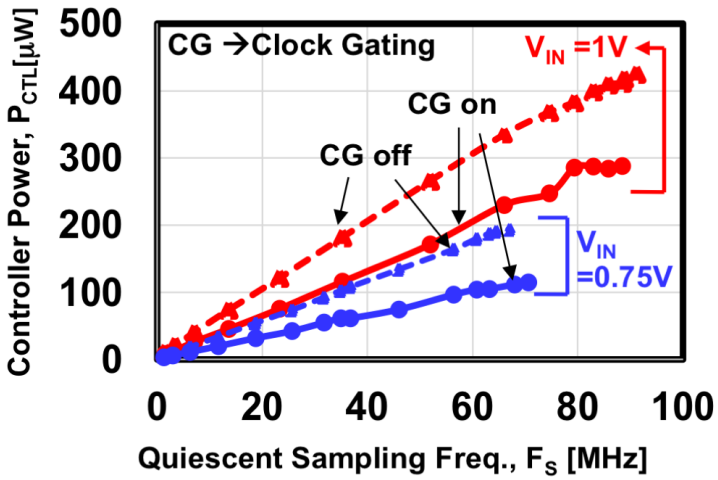


Figure 3.17: Measured controller power reduction with clock gating.

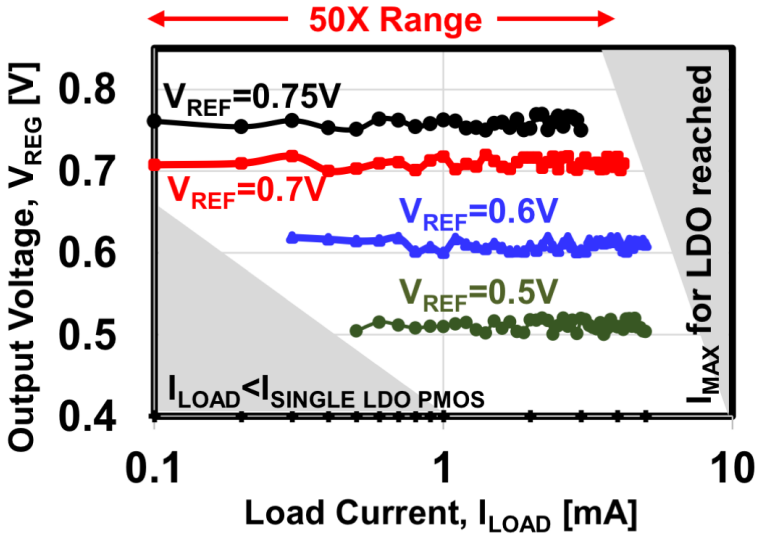


Figure 3.18: Measured load regulation. The steady state ripple of ∼10mV limits the measurement of load regulation.

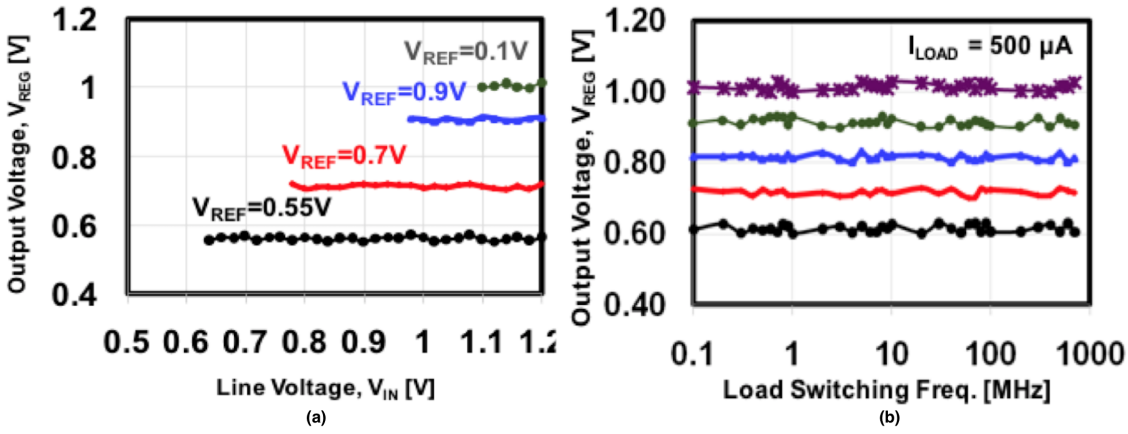


Figure 3.19: (a) Measured line regulation for the LDO design. (b) Measured regulation against load switching frequency. The steady state ripple of ∼10mV limits the measurement of line-regulation and output voltage. The steady state ripple forms a part of the V_{CC} guard-band.

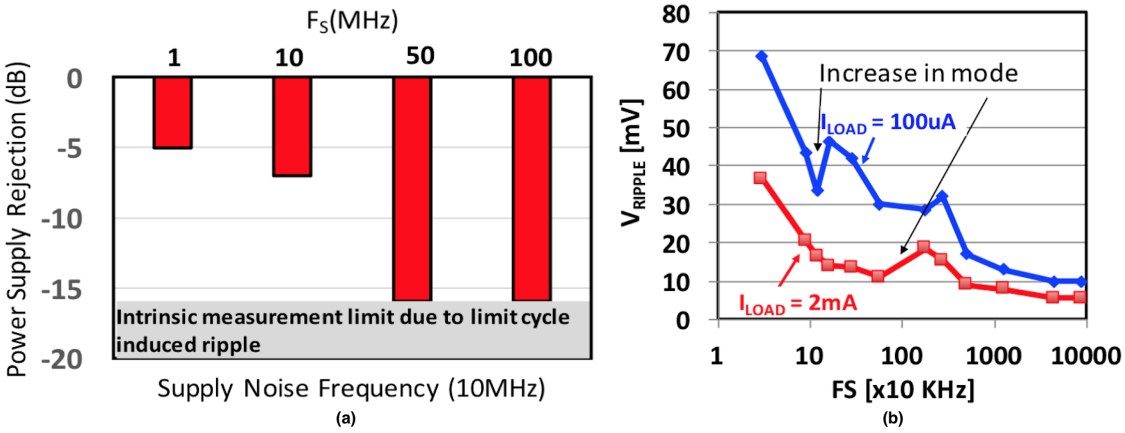


Figure 3.20: (a) Measured supply rejection at 10MHz of supply noise (with a supply ripple of 75mV_{p-p}) as a function of the sampling frequency and (b) Measured voltage ripple (maximum) measured for a wide range of F_S. We note that for low F_S, an increase in F_S causes increase in the mode of oscillation that leads to sudden jumps in the ripple voltage. As F_S increases, the output pole filters out the ripple noise and a residual ripple voltage of 10mV is noted at $F_S \sim$100MHz.

output which is inherent in the design. This does not limit the usefulness of such digital LDOs in powering large digital circuits, as has been demonstrated in [11]. The supply rejection at 100MHz of supply ripple (with p-p ripple of 75mV) shows that an increasing F_S leads to higher loop gain and better supply rejection with a maximum measured rejection of -16dB. This is shown in fig. 3.20a. We also measure the maximum voltage ripple during steady-state as a function of F_S (fig. 3.20b). For low F_S, the ripple is large and we note discrete jumps as the system switches to a higher mode of limit cycle oscillation. This corroborates the theory that is discussed in Section IIB and [21]. With increasing F_S, the output pole tends to filter out the voltage ripple and an inherent ripple of $\sim$10mV is measured at F_S=100MHz. Controller current measured through an ammeter connected between an external power supply and controller supply pins shows a 4x improvement in current efficiency at light load conditions through adaptation when compared to the baseline design (fig. 3.21). A comparative study with recently published data establishes that the current design (Table. 3.1) is competitive in both power efficiency and performance.

A power efficiency figure of merit (FOM_1), defined as the average current efficiency

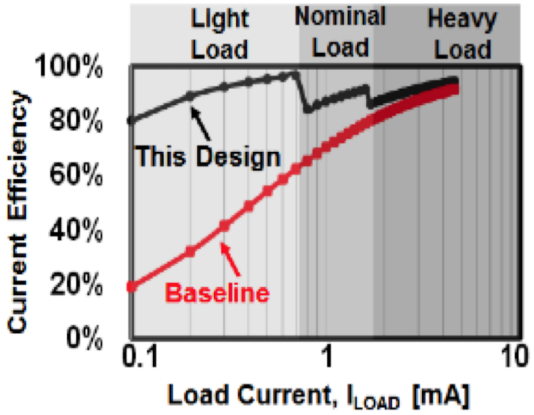


Figure 3.21: Measured current efficiency across the complete load range.

Table 3.1: Measured load regulation, current efficiency and performance.

	This Work	[41]	[18]	[39]
Type	LDO	LDO	LDO	LDO
Technology	130 nm	65 nm	40 nm	45 nm SOI
Control methodology	digital	digital	digital	multiloop Analog
Adaptive Control	Yes	No	No	No
RDS	Yes	No	No	No
Vin (V)	0.5 - 1.2	0.6	0.5	1.179 - 1.625
Vout (V)	0.45 - 1.14	0.4	0.45	0.9 - 1.1
Load Current: I_{max} (mA)	4.6	200	0.2	42
Load Regulation (mV/mA)	<10mV/V*	0.05	0.65	9.8
Line Regulation or Power Supply Rejection	-16dB @ 10MHz	-13dB	3.1mV/V	NA
Controller Current: I_{CTL} (uA)	~ 751	25.1	2.7	9450
Active Area (mm2)	0.114	0.0375	0.042	0.075
Peak Current Efficiency [%]	98.30	99.99	98.70	77.50
Max voltage droop @ Load Step	<40 mV @ 0.7 mA	NA	40 mV @ 200uA	~ 7.6 @ 4.5 mA
FOM1 [%]	90.80%	NA	55.40%	44.90%
FOM2 (process normalized) [ns]	0.036	NA	270	0.0624

FOM1 - Efficiency Metric - Average current efficiency across a 50X current dynamic range

FOM2 - Performance Metric - (Transient Time) * I_{CTL} /I_{max}

* Load regulaltion is below the intrinsic ripple limit of ~10mV/V which is inherent because of the limit cycle oscillations

NA - Insufficient data

across a load range from I_{MAX} to I_{MIN} is $>90\%$, compared to $<56\%$ for previously published data where no load current based adaptation has been shown. RDS, which enables a dynamic trade-off between instantaneous stability and transient response, provides ultra-fast transient response with a discrete-time digital loop, without compromising the runtime stability. FOM_2 [14], normalized to the process node in a manner done in [51], shows that the performance is comparable to its analog counterparts.

CHAPTER 4

MODELING STEADY-STATE DYNAMICS OF A DIGITAL LDO

Although digital LDOs show acceptable transient performance and a wide parameteric design space, but in steady state the regulated output suffers from limit cycle oscillations [18]. In this chapter, we present a nonlinear sampled feedback control model to comprehend the steady state dynamics of a discrete-time digital LDO. The bounds on different modes of limit cycle oscillations under different design parameter constraints are calculated. We propose a dead-zone controller to mitigate these limit cycles and illustrate the parametric design space. The circuit is simulated in a commercial IBM 130nm process design kit (PDK) using H-SPICE and experimental verification is completed through a prototype regulator built on a printed circuit board (PCB) with discrete components.

Section 1 represents the design of the digital LDO (DLDO) in simulation and on the experimental PCB. Section 2 proposes and elaborates the steady state model to capture inherent limit cycle dynamics verified through simulation as well as experiments. It also explores the parametric design space for stability and performance. Finally, a variant of the baseline design is presented in section 3 to mitigate limit cycles. All these sections contain both simulation and hardware measurement results.

4.1 Design of a Discrete-Time Digital LDO

The proposed digital LDO consists of an analog to digital conversion stage which is a single bit comparator in its simplest implementation. It is followed by a programmable gain barrel-shifter which is a variable gain 128-bit shift register with each output bit connected to a power MOSFET. As opposed to a single power MOSFET in analog LDOs, the output power stage is discretized into smaller power MOSFETs (PMOS) as shown in fig. 4.1. In its current implementation, the comparison of output regulated voltage (V_{OUT}) against a

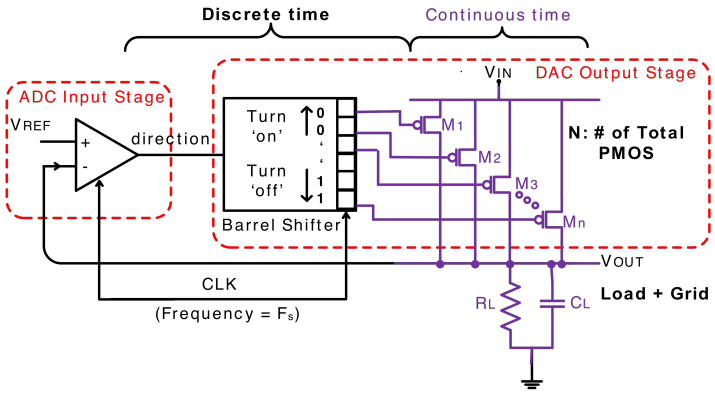


Figure 4.1: Proposed discrete time digital LDO with embedded A/D converter, barrel shifter and a PMOS array.

reference is synchronously obtained through a sense-amplifier based clocked comparator shown in fig. 4.2. This clocked comparator improves power efficiency of the system by obviating the need for a constant bias current in a clock-less version. During the negative phase of the clock, nodes V_a and V_b are charge to Vdd . A discharge race occurs during the positive clock phase and depending on the voltage difference between the two inputs, a decision is latched in a set-reset (SR) latch. The final output is a single-bit bi-directional signal which increments or decrements the barrel shifter output. A programmable range of +3 to -3 shifts is realized through a barrel shifter using two levels of mux presented in fig. 4.3. If $V_{OUT}<V_{REF}$, a certain number of PMOS devices (N_P) are turned on and if $V_{OUT}>V_{REF}$ a certain number of PMOS devices (N_P) are turned off. N_P is obtained from the register-programmable variable gain of the barrel shifter and provides the forward gain of the system (K_{barrel} shifter). In the presented LDO, a variable gain ranging from +3 to -3 (sign represents the direction) is developed in a 128 bit barrel shifter which actuates a total of 51.2μm wide PMOS array capable of delivering a maximum of 3.5 mA at a nominal output voltage of 0.7V from a supply voltage of 1V. The complete circuit is developed and simulated using IBM 130nm process design kit (PDK).

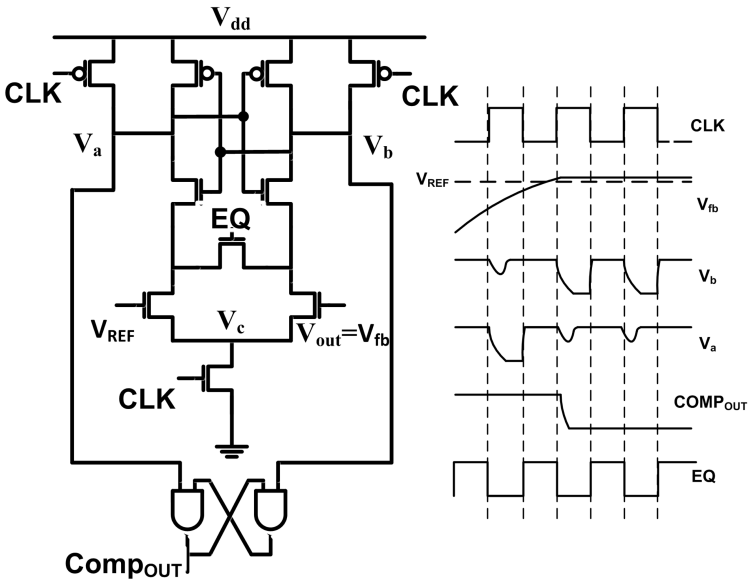


Figure 4.2: Sense amplifier based comparator used as a single bit A/D converter for the proposed LDO.

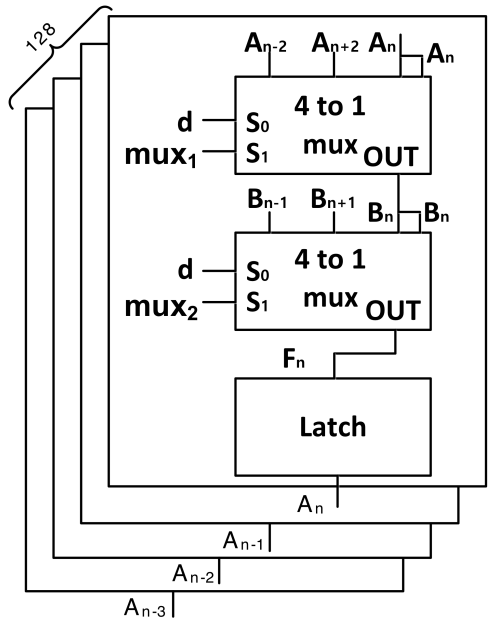


Figure 4.3: Design schematic of a 128-bit barrel shifter using 4x1 mux and latches to provide programmable magnitude and direction of shift. Magnitude of gain is register programmable and the direction is determined by the ADC output.

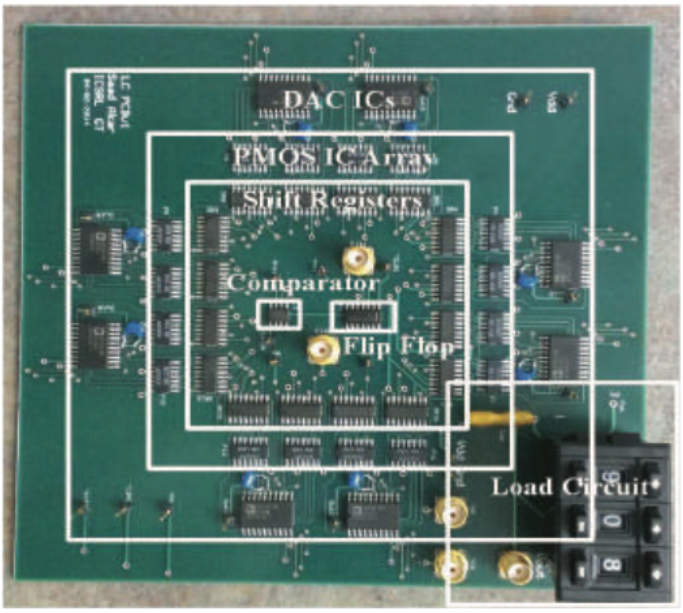


Figure 4.4: Prototype DLDO printed circuit board.

4.1.1 Experimental Setup

An experimental setup using discrete ICs on a printed circuit board (PCB) is developed to validate the digital LDO design, shown in fig. 4.4. An analog comparator followed by a flip-flop acts as a synchronous comparator to realize the ADC stage. A cascade of 8 bit shift registers forms a 64-bit barrel shifter capable of providing a gain of 1 PMOS/cycle. Finally, an array of digital to analog converters (DAC) takes input from gates of the PMOS array. DAC output is a measure of the number of on, off and switching PMOS devices in the array. A programmable potentiometer with a fixed capacitance serves as a variable RC load. Achieved regulation and response to an instantaneous load transient is shown in fig. 4.5 and 4.6 from HSPICE simulation and experimental setup, respectively.

4.2 Steady-state Nonlinear Sampled Feedback Control Model

Increasing the sampling clock frequency (F_s) improves the transient performance of the LDO as shown by the decrease in rise time (T_r) illustrated in fig. 4.7; but it has been shown

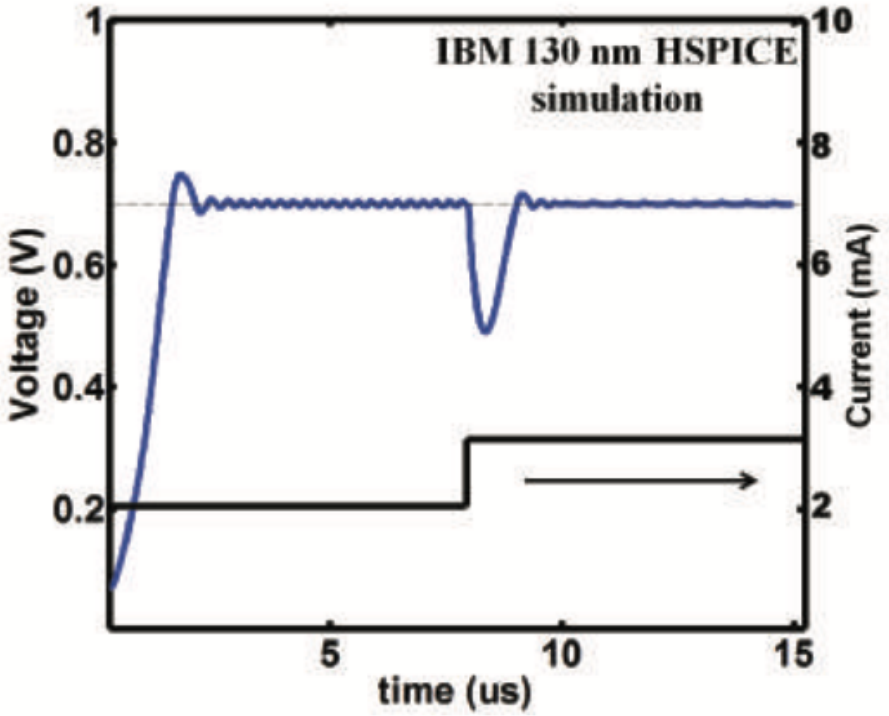


Figure 4.5: Regulation in response to a 1mA load step.

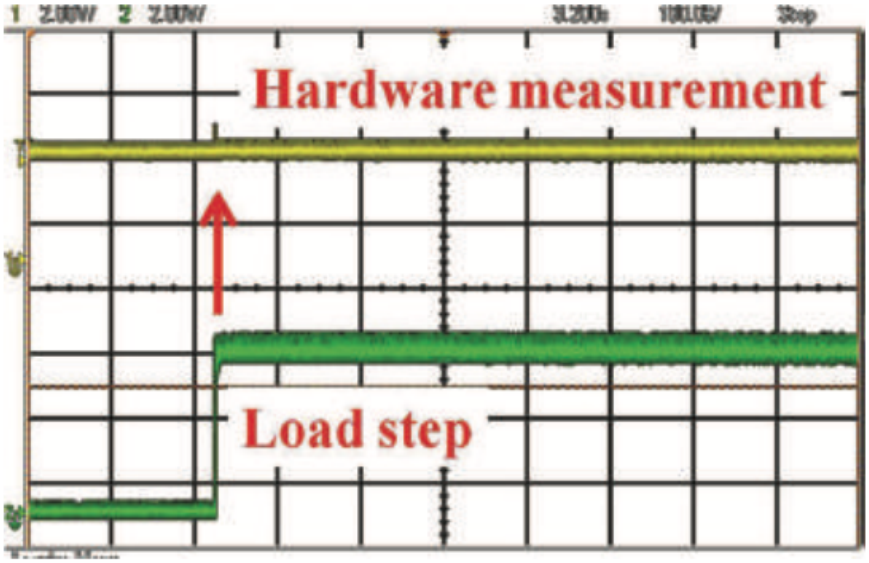


Figure 4.6: Measured load step and regulation on the DLDO PCB.

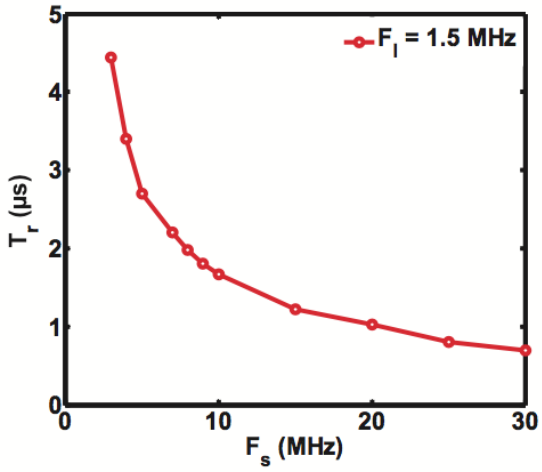
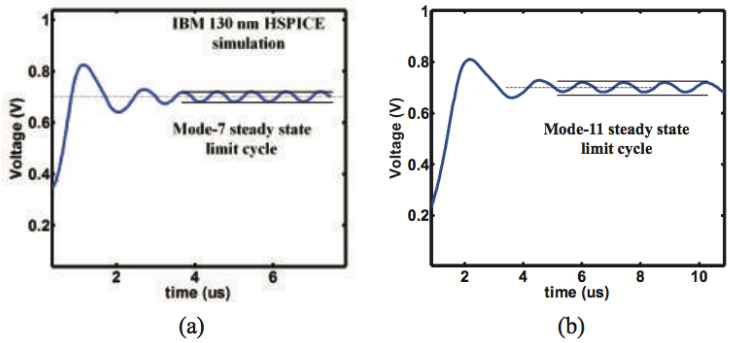


Figure 4.7: Increased transient rise time (0 to 700mV step) performance with increasing F_s.



(a) (b)

Figure 4.8: Steady state ripple shows the existence of (a) mode-7 and (b) mode-11 limit cycle oscillations.

to cause instability in the overall system dynamics if F_s is too high [49]. Therefore, the role of F_s has to be qualitatively and quantitatively understood to ensure a reliable and stable steady state response. Due to the inherent on-off control mechanism of a digital LDO, a number of PMOS devices, called mode hereafter, switch periodically in the steady state and give rise to limit cycles at the output. Fig. 4.8 confirms this oscillatory behavior of V_{OUT} through simulation results. Changing sampling or the load frequency changes the mode of oscillation in the steady state. This behavior is verified through experiments where a change in mode is observed using an array of DACs on the experimental PCB shown in fig. 4.9. A linearized model at the operating point is insufficient in capturing these

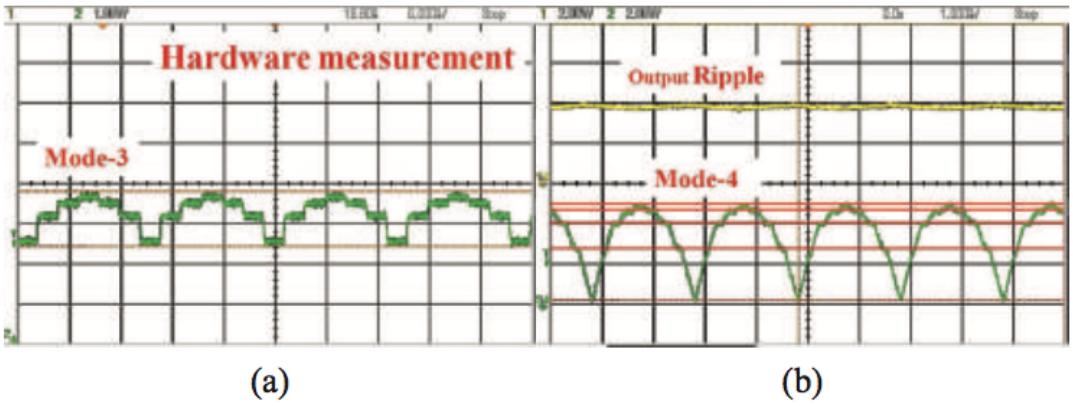


Figure 4.9: Measured output of DACs showing the existence of (a) mode-3 and (b) mode-4 oscillations. $F_s/F_l<3$ for both the measured scenarios.

oscillations; therefore, to accurately quantify the possible modes of limit cycle oscillations, a steady state nonlinear sampled feedback model is developed, as shown in fig. 4.10. The comparator exhibits the characteristics of an ideal relay with zero dead-time if any offset is neglected. It is followed by an impulse sampler running at F_s modeling the ADC stage. Synchronous triggering of the following barrel shifter adds a clock cycle delay in the forward path. Since the barrel shifter accumulated the voltage error over clock cycles, it acts like an ideal integrator. As the number of on PMOS remains constant during the inter-sample period, the conversion of digital samples to continuous-time is modeled by a zero order hold (ZOH). Finally, this number goes through a control to output transfer function, thus converting the digital output of the barrel shifter to a resultant current through the PMOS array (current of each PMOS device = I_{PMOS}). This current actuates the load circuit. The plant is modeled as a first-order low pass filter of the output RC load with a pole at frequency F_l.

4.2.1 Model Development

A limit cycle induces a repetitive pattern at the output of the relay which gives a specific V_{OUT} ripple frequency for each mode. The bounds on a given mode n in terms of $\frac{F_s}{F_l}$ is

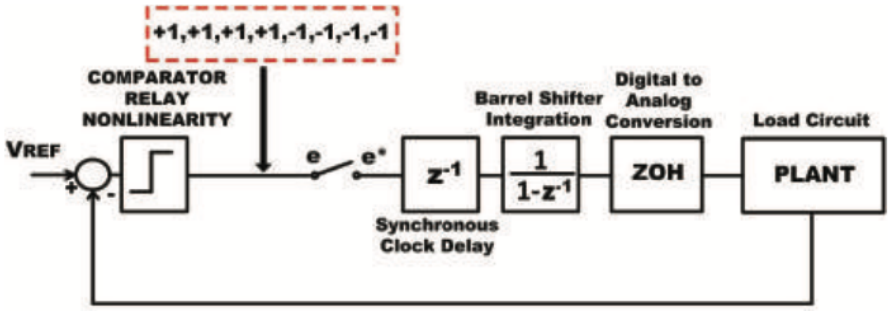


Figure 4.10: Steady state model of the proposed LDO with ideal relay, a delay, an integrator and a sample and hold (ZOH) followed by the load plant.

obtained by applying the Nyquist criterion on the feedback system evaluated at an induced ripple frequency of $\omega_s/(2n)$. Then for n number of PMOS to switch in steady state, a mode-n oscillation is obtained if (4.1) is satisfied.

$$N(A,\phi)L(j\omega_s/2n) = -1 \tag{4.1}$$

Here $N(A,\phi)$ represent the transfer characteristics of hard relay non-linearity and $L(j\omega_s/2n)$ represents rest of the linear components in both the feed forward and feedback portions. Describing function (DF) analysis is used to linearize the nonlinear relay [52]. Application of DF analysis requires a single monotone as input to the relay. In our case, this is validated by the low pass filtering effect of the plant with F_s at least 5-10 times higher than F_l. $N(A,\phi)$ is obtained at a particular frequency given by the following expression

$$N(A,\phi) = \frac{phasor(relay_{OUTPUT})}{phasor(relay_{INPUT})} = \frac{Y'(t)}{x(t)} \tag{4.2}$$

For mode-n to exist, the comparator makes a total of 2n decisions on n PMOS running at F_s. This is equivalent to an input sinusoid of frequency $\omega_s/2n$ to the relay given as

$$x(t) = Asin(\frac{\omega_s}{2n}t + \phi); 0 < \phi < \frac{180^\circ}{n} \tag{4.3}$$

All the switching PMOS at least switch once in 180°. Since output of the relay is in terms of discrete samples, the fundamental component of it is advanced in phase by $(180/2n)^\circ$

$$|Y'(t)| = \frac{2}{nT}\int_0^n Ty'(t)sin(\frac{\omega_s}{2n}t + \frac{180^\circ}{2n})dt \tag{4.4}$$

This integration is solved by a direct summation of the samples evaluated at time T_s and $\omega_s = 2\pi/T_s$; For samples of amplitude M, this simplifies to

$$|Y'(t)| = \frac{2M}{nT}\sum_0^n sin(\frac{2\pi}{2n}t + \frac{180^\circ}{2n}) \tag{4.5}$$

Evaluating 4.2 using 4.3 and 4.5 gives

$$N(A,\phi) = \frac{\frac{2M}{nT}\sum_0^n sin(\frac{2\pi}{2n}t + \frac{180^\circ}{2n})}{Asin(\frac{\omega_s}{2n}t + \phi)} \tag{4.6}$$

As an example, mode-2 evaluates to

$$N(A,\phi) = \frac{\sqrt{2}M}{TA}\angle 45^\circ - \phi; 0 < \phi < 90^\circ \tag{4.7}$$

and mode-3 gives

$$N(A,\phi) = \frac{\sqrt{4}M}{3TA}\angle 30^\circ - \phi; 0 < \phi < 60^\circ \tag{4.8}$$

The response function of rest of the linear portion comprises of cascaded transfer functions given as

$$L(j\omega) = H(j\omega)Z(j\omega)S(j\omega) \tag{4.9}$$

Here S represents the discrete integration with sampling delay, Z represents ZOH and H is the plant transfer function. Evaluating 4.9 at $(\omega_s/2n)$ gives

$$L(\frac{j\omega_s}{2n}) = \frac{e^{-j\frac{\omega_s}{2n}T}\angle -tan^{-1}(\frac{\omega_s\tau}{2n})}{j\frac{\omega_s}{2n}\sqrt{1+\frac{\omega_s\tau}{n}^2}} \tag{4.10}$$

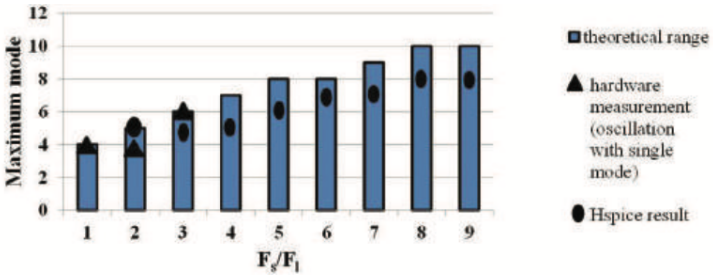


Figure 4.11: Possible modes for increasing F_s/F_l with simulation and experimental results superimposed.

Using 4.6 and 4.10 in 4.1 gives

$$-1 = \frac{\frac{2M}{nT}\sum_0^n sin(\frac{2\pi}{2n}t + \frac{180o}{2n})}{Asin(\frac{\omega_s}{2n}t + \phi)} \frac{e^{-j\frac{\omega_s}{2n}T} \angle -tan^{-1}(\frac{\omega_s\tau}{2n})}{j\frac{\omega_s}{2n}\sqrt{1 + \frac{\omega_s\tau}{n}^2}} \tag{4.11}$$

Finally, the linearized response function is evaluated using 4.11 which gives the bound on F_s/F_l ratio for mode-n. As an example, mode-3 simplifies to

$$-tan^{-1}\frac{\tau\pi}{3T} - 60^\circ - 90^\circ + 30^\circ - \phi = -180^\circ \tag{4.12}$$

$$\frac{\tau\pi}{3T} = tan(60^\circ - \phi) \tag{4.13}$$

$$0 < \frac{F_s}{F_l} < 1.65; 0 < \phi < 60^\circ \tag{4.14}$$

Total feed forward gain per cycle is given by $K = K_{barrel}I_{pmos}$ and $\tau = 1/F_l$. Fig. 4.11 summarizes the accuracy of the obtained model compared with simulation and experimental results. The highlighted regions shows the possibility of existence of a given mode at a certain F_s/F_l value. The dynamic range of experimental setup allows verification till F_s/F_l=3. The above analysis can capture F_s/F_l bounds for any equivalent design changes in the feedback loop following the exact analysis presented in this section. These bounds represent the necessary conditions for a limit cycle to exist but may not be sufficient as amplitude condition in Nyquist criterion also needs to be satisfied. If multiple modes are possible for

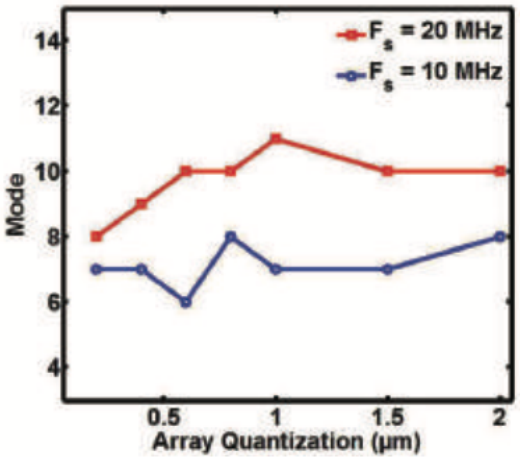


Figure 4.12: Lmit cycle modes with increasing PMOS array quantization at two different F_s.

a given F_s/F_l value, then the exact oscillation mode is determined by the forward gain in the loop which is highly non-linear since a digital LDO output PMOS array is not biased as current sources but rather switches with low gain but small on resistance. Nevertheless, the theoretical model gives us the worst-case bounds of limit cycle oscillations against F_s/F_l values.

4.2.2 The Role of Quantization of the PMOS Array

The size of each PMOS in the array plays an important role in determining the overall forward path gain. It should be noted that an increase in the output ripple does not necessarily mean an increase in mode. Following the amplitude requirement imposed on the existence of a limit cycle by 4.11, an increase in I_{PMOS}, with larger size of each PMOS of the array, results in an increase in the forward path gain. This increases the V_{OUT} ripple even though the steady-state mode may only undergo negligible increase as verified by fig. 4.12. Due to second order effects in I_dV_{sd} characteristics of the PMOS array, the gain is non-linear and can be quantified through numerical simulations. Since there are a number of possible modes of oscillations, the exact mode of oscillation in which the loop settles down under given load conditions is a function of the forward-path gain. This trend is valid if F_s/F_l is

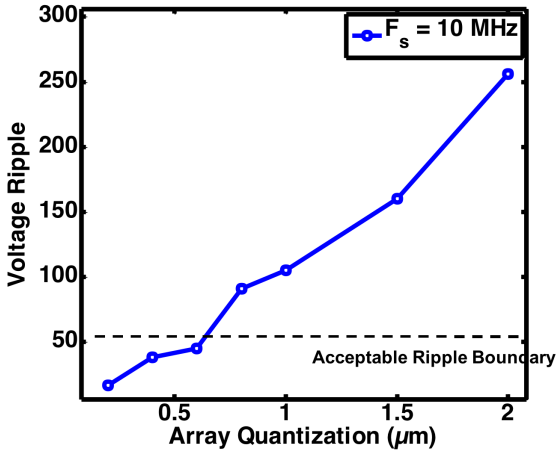


Figure 4.13: Increasing ripple with larger PMOS array quantization.

not large. The overall array size is determined by the current requirements of the underlying load; whereas, the array quantization is set by the ripple specification. For the current design, a width of 750nm of each PMOS gives a maximum gain while remaining within the ripple bound at a maximum specified F_s/F_l as depicted in fig. 4.13.

Similarly, increasing the capacitance at the output decreases output ripple but F_l decreases as well. This causes an increase in the mode of oscillation which may increase the steady state ripple. Although the two trends oppose each other but ultimately ripple changes the drop-out on the PMOS array which determines the forward gain. A lower ripple translates into an overall lower loop gain which prevents further increase in the mode.

It should also be mentioned that the overall DLDO loop presents two distinct quantization stages. The first one is the input sampling stage, where a clocked comparator presents a hard quantization of the sampled input. The output stage, consisting of the PMOS array presents the second quantization. Since the number of quantization levels available at the output is significantly higher than at the input, the quantization noise introduced at the input by the comparator dominates the overall non-linearity in the loop. Hence, it is not surprising that the sampling frequency plays a significant role in the limit cycle dynamics, whereas the PMOS array has a less prominent role in determining the mode of limit cycle oscillations under a realistic size of each PMOS in the array.

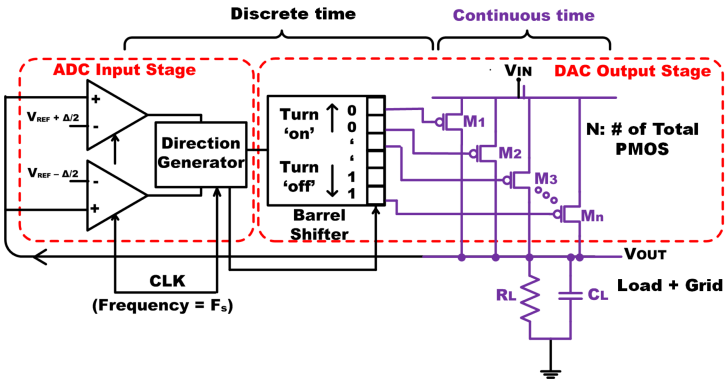


Figure 4.14: Proposed variant of baseline DLDO with dead-zone A/D converter, barrel shifter and a PMOS array.

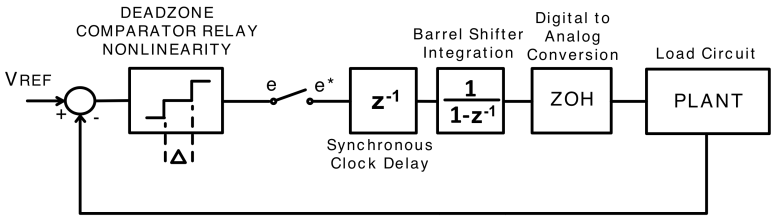


Figure 4.15: Steady-state model for the digital LDO with deadzone.

4.3 Dead-zone Controller for Reduced Steady-state Ripple

The gain provided by the relay based non-linearity is a function of both amplitude and phase of the input sampled signal. Decreasing this gain enhances the stability of the system which results in reducing or eliminating the limit cycle oscillations. This can be achieved by introducing a dead-zone in the comparator stage by using two comparators in tandem, followed by a shift logic block that produces the direction as well as a clock enable for the barrel shifter. Fig. 4.14 gives the detailed system level design of the dead-zone DLDO. The two clocked comparators in the ADC stage can provide both a symmetric and non-symmetric dead-zone around V_{REF} . Shift logic in the barrel shifter is temporarily disabled when V_{OUT} is within the dead-zone. This not only helps in removing the steady state oscillations but also saves dynamic power consumed in a continuously clocked barrel shifter. An equivalent steady state model, devised following the same procedure adopted before, is shown in fig. 4.15. A relay with dead-zone captures the steady state dynamics of the two

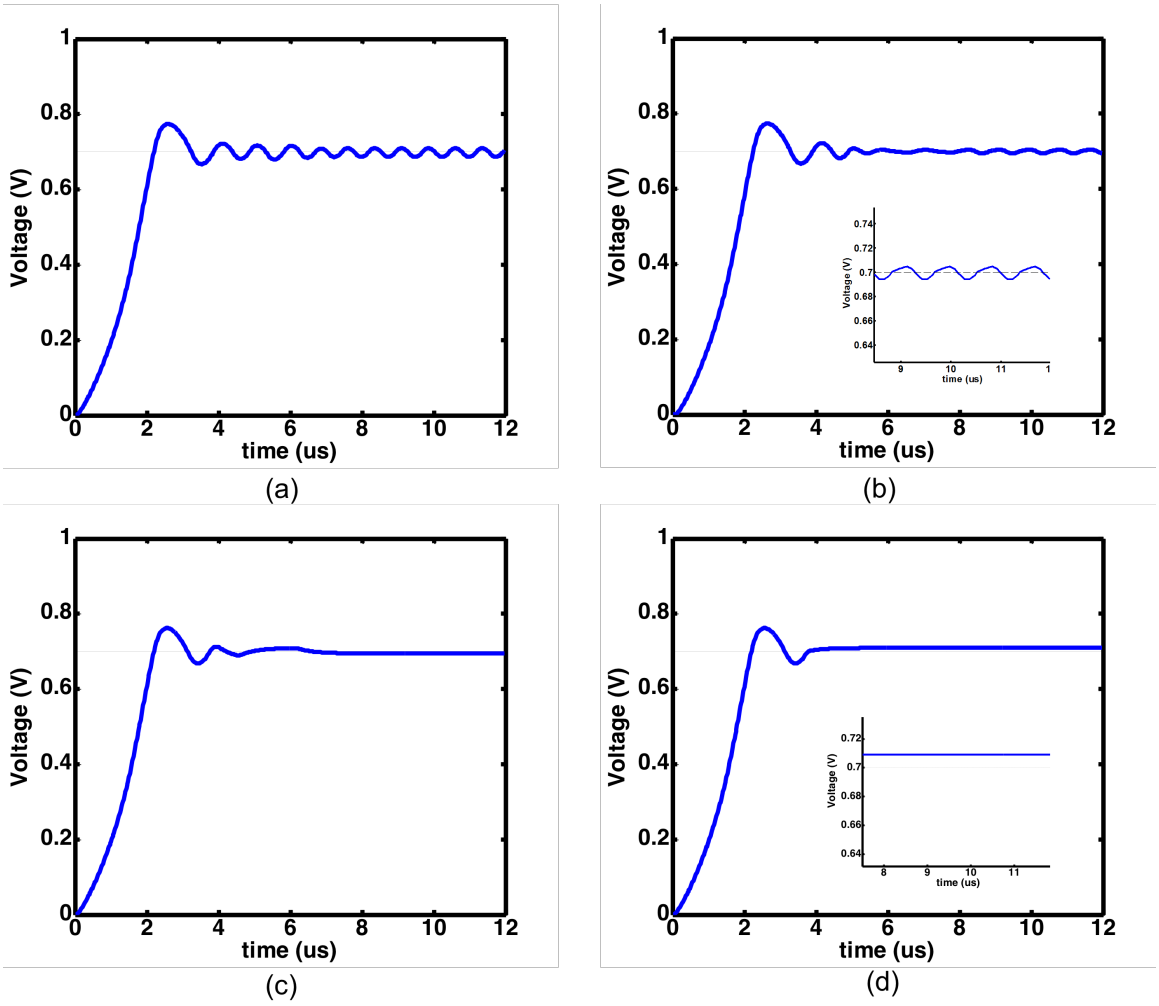


Figure 4.16: Increasing dead-zone (a-d) removes steady state oscillations at the cost of the accuracy of DC regulation.

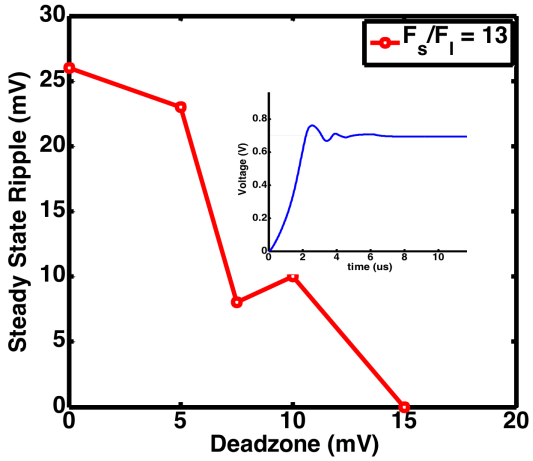


Figure 4.17: Trend of decreasing steady state voltage ripple with increasing dead-zone.

comparator ADC stages. The summation of samples in 4.6 during the dead-zone results in zero. Therefore, the forward-path gain is reduced as the size of dead-zone increases ($K_{forward}\alpha 1/\Delta$). This helps to remove the limit cycle oscillations as illustrated by simulation graphs in fig. 4.16 and 4.17. However this limits accuracy of the DC load and line regulation, and the accuracy decreases for increasing the dead-zone voltage. Thus the dead-zone provides a design trade-off between the steady-state output ripple and the steady-state error (i.e., the difference between V_{REF} and V_{OUT}) and also acts as a powerful knob to increase current efficiency of the regulator under suitable load conditions where a bounded steady-state error is tolerable.

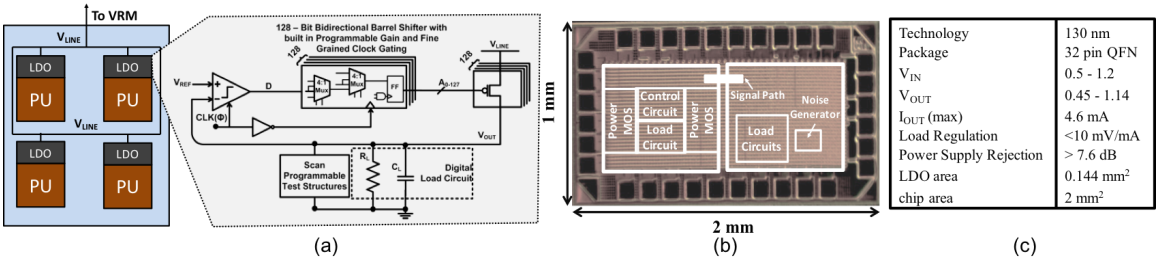
CHAPTER 5

PROACTIVE CONTROL OF DIGITAL LDO

Run-time adaptation knobs of operational frequency and power transistor quantization size in a digital LDO allow us the opportunity to instantaneously change the operational capability of the LDO. Such knobs can be controlled through software or hardware to provide a wide operational range. It allows us to achieve optimum balance of power and performance across power saving and high performance modes of digital load circuits.

In this chapter, we explore through simulations and measurements (test-chip micrograph shown in fig. 5.1), the notion of gain-boosting through run-time operational frequency tuning in a digital regulator with reactive and proactive control, to minimize droops during large load steps. The major contributions of this part of the thesis are (a) Measured demonstration of the effectiveness of proactive software control to enhance LDO transient performance under large voltage droops and (b) PSR modeling of all-digital LDOs and gain boosting to enhance PSR performance against supply noise.

The design and general trade-offs of an all-digital linear regulator are reviewed in Section 1. A comparison of reactive and proactive control for mitigating power supply rejection is carried out in Section 2. Section 3 presents a power supply rejection model used to analyze the underlying regulator and performance adaptation through gain boosting. Both



Technology	130 nm
Package	32 pin QFN
V_{IN}	0.5 - 1.2
V_{OUT}	0.45 - 1.14
I_{OUT} (max)	4.6 mA
Load Regulation	<10 mV/mA
Power Supply Rejection	> 7.6 dB
LDO area	0.144 mm^2
chip area	2 mm^2

Figure 5.1: (a) Multiple on-chip power domains with embedded point-of-load digital LDOs. (b) Chip micrograph showing two voltage domains. (c) Chip specification table

Section 2 and 3 provide measurement results from the test chip.

5.1 Baseline Design

A dual clock edge all-digital LDO is presented in fig. 5.1a. The design consists of a digital control section comprising of a clocked comparator followed by a shift register and an array of 128 controlled PMOS pass devices. The second-order closed loop gain of the LDO is a function of the sampling clock frequency (F_S), as has been discussed extensively in previous chapters. The design of the LDO follows the same topology as described in chapter 4. An increasing F_S (relative to the location of the output pole, F_{LOAD}=1/(k.R_{LOAD}.C_{LOAD})), takes the system from an over-damped to underdamped response. Further, the hard quantization of the comparator and the finite quantization of the PMOS array introduce steady-state limit cycle oscillations and hence an output ripple, which is a hallmark of digital regulators. A higher F_S increases the limit cycle oscillation which can lead to higher steady-state ripple; hence, the ratio of F_S/F_{LOAD} needs to be bounded. In the current design a nominal F_S ($F_{NOMINAL}$) of 20MHz was selected. Since F_S plays a critical role in the overall closed-loop gain of the system, it also provides a unique opportunity to enable real-time and almost instantaneous gain boosting in a digital regulator in response to a large load step. In this chapter, we explore such a paradigm through measurements on a silicon chip fabricated in a CMOS 130nm IBM process (fig. 5.1b, c) and demonstrate the efficacy of gain boosting in digital regulators. Clock gating, an effective method of power saving in digital load circuits, is commonly used in industrial designs. However, going into (coming out of) a clock gated mode from (to) normal operation, creates very large load transients and lead to large overshoots (voltage droops) in the logic circuit (fig. 5.2a). The corresponding response time of the supply regulator, hence, is critical, and limits how often clock gating can be employed.

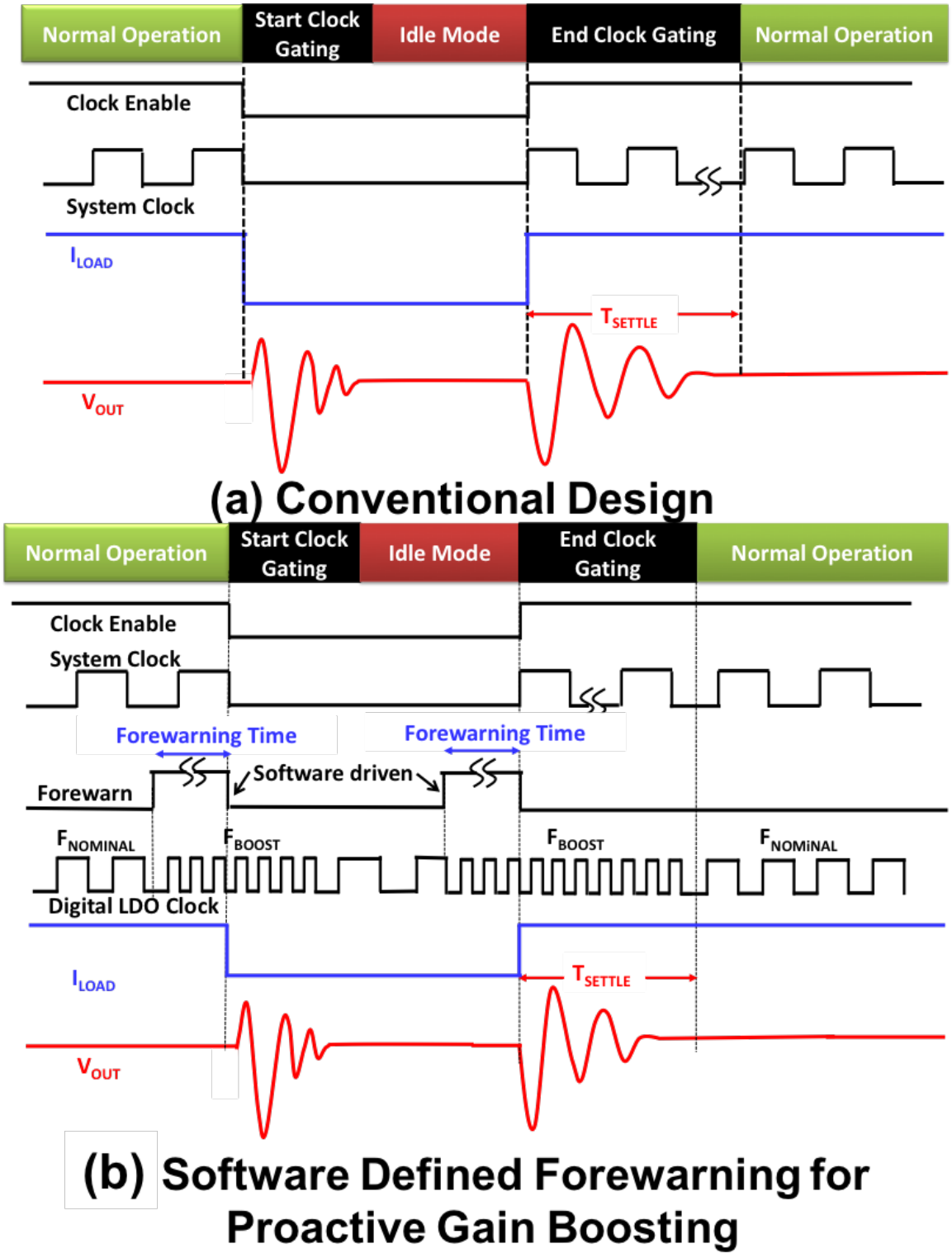


Figure 5.2: (a) Conventional design showing supply droops/overshoots in response to clock gating/un-gating. (b) Forewarning signal provides proactive gain boosting in digital regulators.

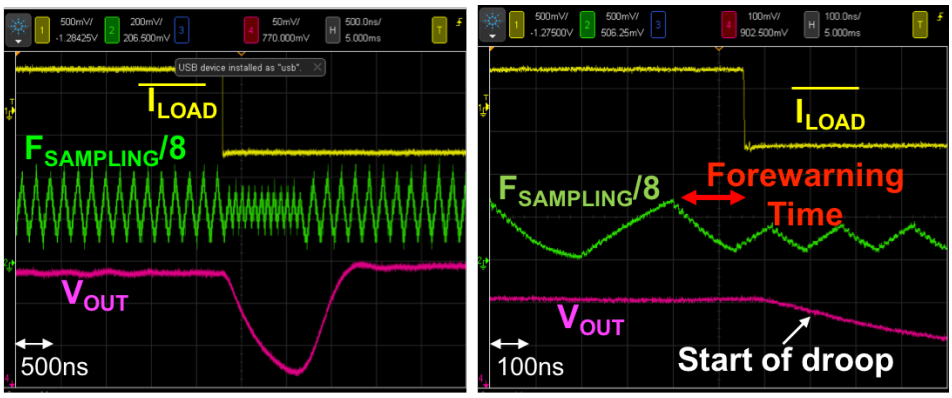


Figure 5.3: Oscilloscope captures showing purely reactive and proactive gain boosting under iso-load steps (2mA step). Here $F_{SAMPLING}$=F_S has a nominal value of 20MHz.

5.2 Proactive vs Reactive Control

In traditional design, regulators (analog or digital) are feedback circuits that react to changes in the output voltage by regulating the current to the load. A higher closed loop gain (within the bounds of stability) can achieve faster regulation. Unlike analog regulators, in a digital regulator, the loop dynamics (particularly gain and system poles) can be controlled by F_S, and sudden current demands can be satisfied by gain-boosting even at low currents (voltages). In our design, gain boosting is achieved by employing an undershoot and overshoot detector which compares the output voltage with $V_{REF}\pm\Delta$ such that whenever an undershoot or overshoot is detected, a higher F_S is employed and a faster recovery and lower supply droop/overshoot is achieved at iso-load step (fig. 5.3).

Test-chip measurements of such a reactive scheme demonstrate significant improvements in both the transient time and magnitude of the droop for different values of Δ, for two different values of the boosted regulator frequency (F_{BOOST}) (fig. 5.4a, b). As opposed to this purely reactive scheme, a load-regulator co-design can enable a proactive approach in droop mitigation. In most digital designs, information about large transient events, like clock gating/un-gating is available a few clock cycles in advance from the mi-

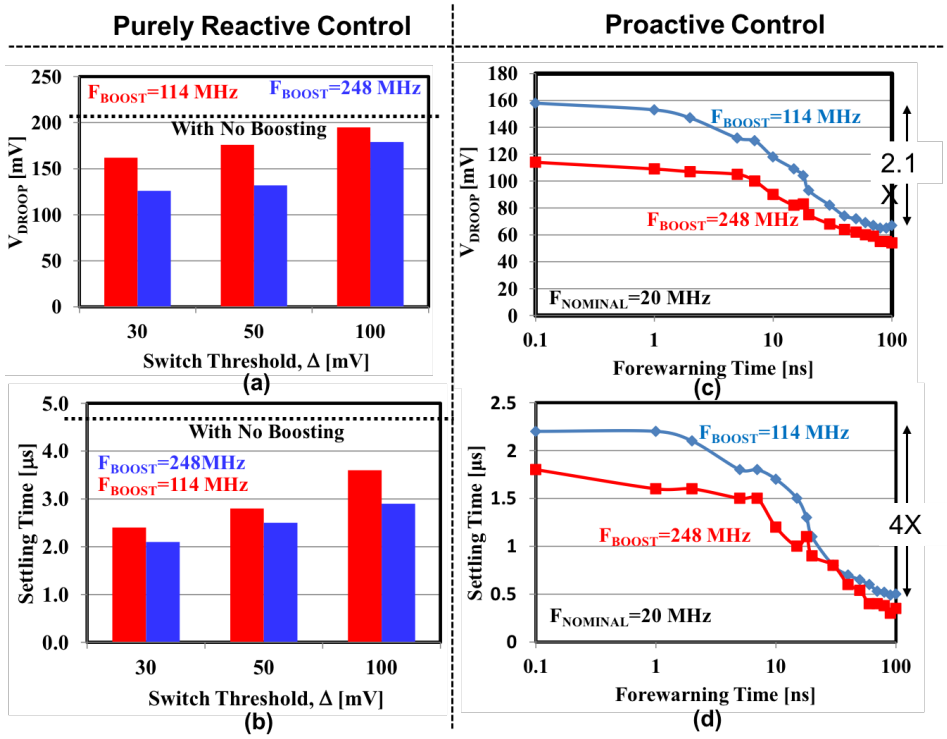


Figure 5.4: (a,b) Measured droop reduction and settling time for reactive control. (c,d) Measured droop reduction and settling time at iso load-step conditions. The nominal F_S is called $F_{NOMINAL}$.

croarchitecture/software stack [53]. Clock gating during a cache miss in a microprocessor, or refreshing a display in a mobile device are examples of workloads with very predictable and deterministic clock gating/un-gating patterns. Since the microarchitecture state is expected to have visibility into the system over several clock cycles, a forewarning signal can be issued before the actual clock gating/un-gating is enabled. Such a forewarning signal can be propagated to the digital LDO in a feed-forward path. It can, then, allow the regulator to preemptively switch to higher gain, to reduce an impending voltage droop. The earlier this warning signal is propagated to the LDO, the lesser the droop and the settling times are (fig. 5.4c,d). From silicon measurements, we note a saturating trend when the warning signal is available more than 100ns in advance. We see large benefits with a forewarning signal that arrives 10ns-100ns before the actual load step, which is equivalent to 10-100 clock cycles in a 1GHz processor and is in the realm of prediction from the microarchitecture [53].

5.3 Power Supply Noise Rejection and Gain-boosting to Reduce Cross-domain Supply Noise

In digital linear regulators, the power MOSFETs operate in a linear or triode region. This leads to a lower power supply rejection (PSR), which is typically an acceptable trade-off in digital load circuits. However, this leads to cross-domain noise coupling where supply noise of a local grid can propagate through a shared voltage line (fig. 5.1) to adjacent grids. In this section, we demonstrate (through theory and measurements) that the poor PSR in digital LDOs can be compensated for by proactive gain boosting in adjacent (victim) power grids when a large load transient in expected in an aggressor power grid. A behavioral model to explain PSR can be best approximated in the steady state where all the on switches of the PMOS array are contributing equal current to the output under a constant drop-out voltage. Under such conditions, following the PSR shunt model of [54], we can model the Z_{OUT} at the output of the LDO as a parallel combination of shunt ($\approx Z_{OUT}/loopgain(LG)$) and load impedance. Increasing F_S increases LG which lowers the shunt impedance and steers the noise current away from the load. At a decreased F_S, the effect of shunting impedance is reduced which decreases the closed loop gain and lowers the PSR.

5.3.1 Power Supply Rejection Model

In this subsection, we provide a mathematical framework which establishes the effect of increasing F_S on the power supply noise rejection performance of a digital LDO. With a constant feedback factor (=1) and load (F_{LOAD}), following the analysis carried out in chapter 3, LG of the LDO in z-domain is given as

$$LG(z) = \frac{K(1 - e^{-F_{LOAD}/F_S})}{(z-1)(z - e^{-F_{LOAD}/F_S})} \tag{5.1}$$

Here K comes out to be a constant of proportionality which represents the gain of PMOS devices. Under the constraint that F_S is at least 5 to 10 times higher than F_{LOAD}, a z to s

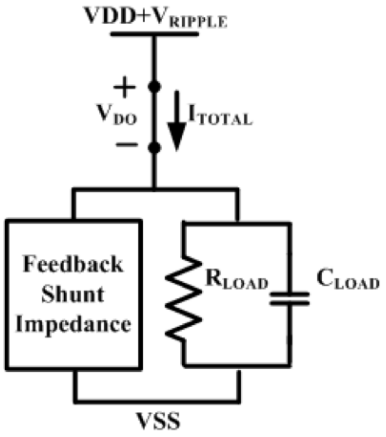


Figure 5.5: PSR model showing shunt feedback path.

domain transformation is carried out using:

$$z = 1 + sT_S \tag{5.2}$$

where $T_S = 1/F_S$. Putting (5.2) in (5.1) gives

$$LG(s) = \frac{K(1 - e^{-F_{LOAD}/F_S})}{(sT_S)(1 + sT_S - e^{-F_{LOAD}/F_S})} \tag{5.3}$$

$$LG(s) = \frac{K}{(sT_S)(1 + \frac{sT_S}{1-e^{-F_{LOAD}/F_S}})} \tag{5.4}$$

By Taylor expansion and neglecting higher order terms, $e^{-F_{LOAD}T_S} \approx 1 - F_{LOAD}T_S$. Then (5.4) can be written as

$$LG(s) = \frac{K}{(sT_S)(1 + \frac{s}{F_{LOAD}})} \tag{5.5}$$

PSR analysis is divided in to two different frequency regions.

Region I: In the first region $s > 2\pi F_{LOAD}$ and Region II: where $s < 2\pi F_{LOAD}$. Following fig. 5.5 [6], impedance looking downward into the load at the regulated output voltage is given as:

$$Z_{PD} = Z_{LOAD}||Z_{SHUNT} \tag{5.6}$$

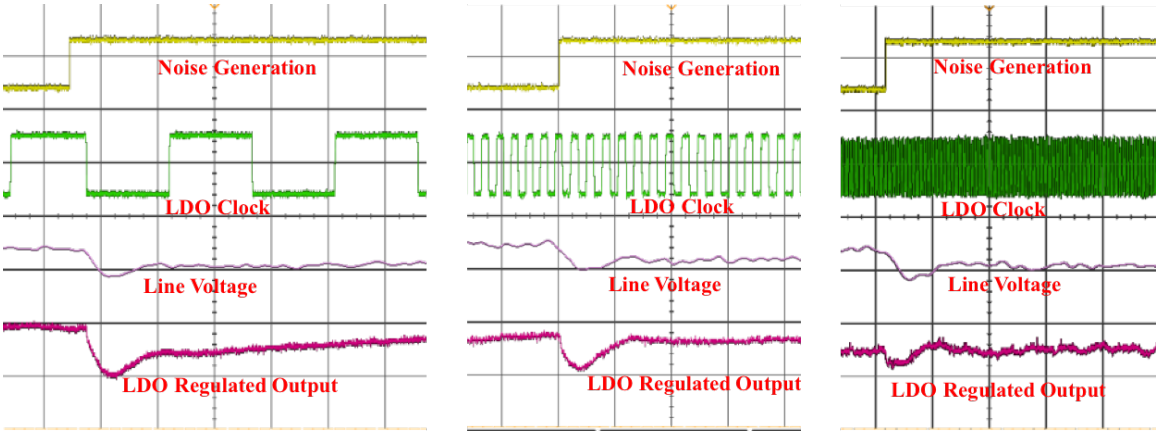


Figure 5.6: Improved PSR with increasing clock frequency

$$Z_{PD} = \frac{R_{LOAD}}{1 + \frac{s}{F_{LOAD}}} || \frac{(\frac{R_{LOAD}}{1+\frac{s}{F_{LOAD}}} || \frac{V_{DROPOUT}}{I_{LOAD}})}{LG} \tag{5.7}$$

In region I, value of LG is small as can be inferred from (5.5), therefore; Z_{PD} is dominated by the output pole. In this region, C_{LOAD} dictates the PSR value. In region II, equation (5.5) is used in (5.7) under the assumption that $s << 2\pi F_{LOAD}$. It results in the following simplified form of pull down impedance:

$$Z_{PD} = R_{LOAD} || ((\frac{V_{DO}}{KV_{DD}}(sT_S)R_{LOAD}) \tag{5.8}$$

From (5.8), it can be clearly inferred that with decreasing T_S, Z_{SHUNT} becomes smaller than Z_{LOAD} and shunts away the ripple current coming to the regulated output node from the supply. The overall PSR of the system is given as:

$$Z_{PD} = \frac{Z_{PD}}{Z_{PD} + R_{DO}} \tag{5.9}$$

which shows that decreasing Z_{PD} improves power supply rejection near DC at low frequencies by using a higher F_S as measured in fig. 5.6. The improvement in PSR in a pro-active manner is further corroborated through measurements in the following section.

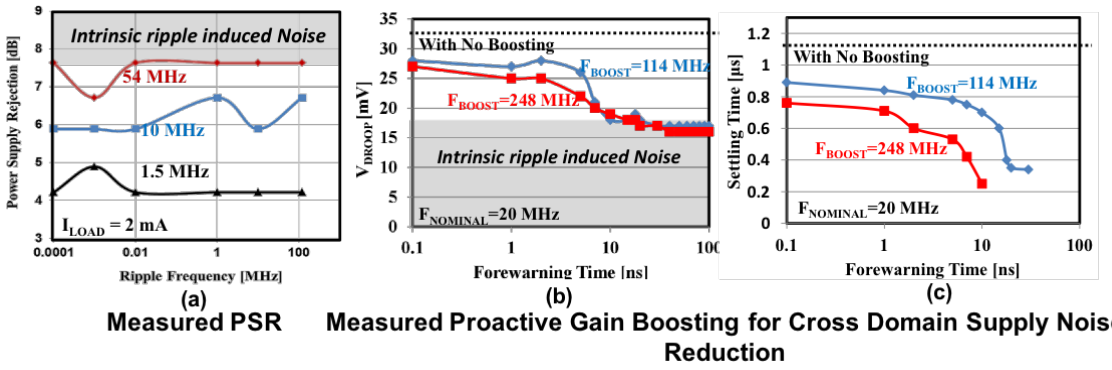


Figure 5.7: (a) Measured PSR as a function of ripple and sampling frequencies. (b,c) Measured voltage droop and settling time as a function of the forewarning time.

5.3.2 Cross Domain Proactive Regulation

With an injected supply noise of 85mV$_{p\text{-}p}$, a measured PSR of 7.61dB is achieved when the system is running at an F_S of 54MHz and I_{LOAD} of 2mA (fig. 5.7a). As F_s is further increased the output noise falls below the noise floor caused by the steady state ripple. An unwanted consequence of this, in a multi-core processor, is that load transients (due to clock gating/un-gating) from one core can cause large voltage fluctuations in the shared incoming voltage grid. The noise predominantly spreads at the resonant frequencies of the LC section of the package and the package to chip interface. Due to the poor PSR of digital linear regulators, a large portion of the noise can couple into adjacent cores (which are running workloads) creating timing errors. The availability of a forewarning signal before clock gating/un-gating can also be propagated to adjacent voltage grids to temporarily boost the local regulator clock (F_S) and provide an instantaneous boost in the PSR. This opportunistic PSR adaptation comes at a minimal cost of increasing F_S only during large load transitions. It reduces the magnitude of the coupled noise and time to recover from the noise. With warning signal propagated 10ns in advance to a noise event occurring in an adjacent load, the proactive gain boosting achieves a 3x decrease in settling time and a 2x decrease in voltage droop magnitude. If the forewarning signal is available well in advanced ($> 10ns$) the transient performance of gain boosting saturates since the system is already operating at

its highest rated performance. The measured results from the test chip showing the efficacy of this run time adaptation are summarized in fig. 5.7(b,c).

CHAPTER 6

CORE-LEVEL LOAD CURRENT DIGITAL LDO WITH ASYNCHRONOUS NON-LINEAR CONTROL

Up till now, we have explored and designed digital LDOs capable of powering small digital functional units that consume a few milli-amperes of load current. There is a need to scale up the load current capability of digital LDOs to enable optimal voltage regulation of a large voltage domain as expected in an industrial big chip. Thanks to its digital logic synthesis and automated placement and routing, a digital LDO can enable per-core DVFS in large microprocessors and systems-on-chip (SoC) designs at a low design complexity and integration time. To this serve this end, this chapter showcases a digital LDO with load current driving capability of up to 125mA enabling per-core voltage regulation. The design allows maximum digital process flow synthesis, fast asynchronous sensing for transient events and uses nonlinear control to achieve fast voltage droop mitigation.

In its basic form, a digital LDO discretizes both control and power stage by using clock for synchronous sensing and turning on/off small power transistors instead of a single large power transistor [18]. This quantized nature results in an inherent trade-off between the transient and steady-state performance of a digital LDO [23]. A faster sampling clock can improve transient performance against sudden load changes but during steady-state it results in an increased voltage ripple due to limit cycle oscillations [21]. To decouple steady-state response from transient performance, this chapter proposes the use of asynchronously sensing load transients to separate it from steady-state operation. This obviates the need for employing a fast clock to meet a transient specification significantly saving power otherwise, expanded in fast clock generation and distribution. Secondly, to enable ultra-fast voltage droop recovery, we employ non-linear control which results in maximum droop mitigation against large load transients under limited decoupling capacitance budget.

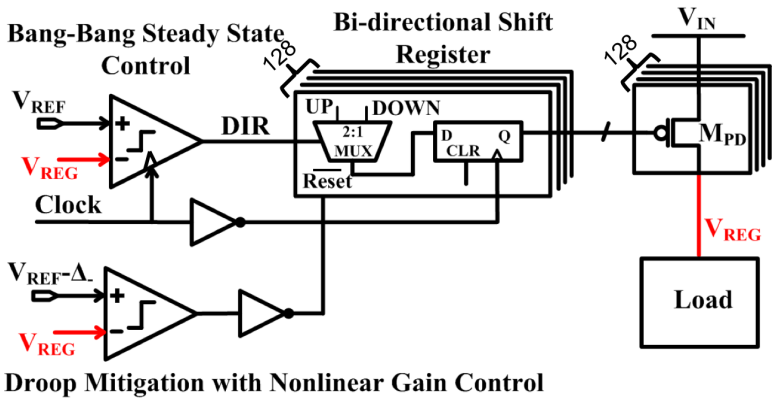


Figure 6.1: Architecture of the proposed digital LDO.

This topology is especially suitable for load circuits that can remain operational when regulated voltage is above or equal to the reference voltage as opposed to just being equal to it. Both asynchronous sensing and nonlinear control are integrated in a basic digital LDO topology to retain a wide operational current and voltage range.

The remaining chapter is written as follows. In section 1, we explain the motivation and operation of asynchronous non-linear control. In section 2, the architecture and design of the digital LDO are presented followed by measurement results from a test-chip built in 65nm CMOS process.

6.1 Motivation and Operation of Asynchronous Non-linear Control

6.1.1 Asynchronous Voltage Droop Detection

The operation of a basic digital LDO utilizes a master clock to sense and actuate power transistors as shown in fig. 6.1. It has been well established that increasing clock frequency at iso-load condition makes the LDO loop underdamped. It results in long settling time after a load transient due to decreased phase margin and a large voltage ripple in steady-state. Ultimately, an unstable behavior or loss of regulation can occur if the clock frequency is increased to a very high value. Therefore, an upper limit on the operational clock frequency limits the maximum achievable transient performance which is of tantamount importance

in digital circuits with small decoupling capacitor budget.

As a solution, voltage droop detection using a clock-less comparator in high performance modes decouples the transient performance of the LDO from the master clock frequency. Biased clock-less comparators can outperform sense amplifier based comparators at high voltages where load transients also exhibit large changes [55] . As the supply voltage goes down, the magnitude of load current steps also decreases and regular droop detection techniques can be employed.

6.1.2 Non-linear Control

In the proposed non-linear control, all the power transistors of the digital LDO are asynchronously turned on when a voltage droop is detected. This results in maximum voltage droop mitigation as compared to any other control action which turns on a lesser number of power transistors. Due to this non-linear droop mitigation, a large mismatch between load and supply current can induce an unfavorable large overshoot. The clamping effect of the power transistors and enough decoupling capacitor on the supply node will keep the overshoot equal or below the supply voltage.

Nevertheless, this nonlinear action results in extra power losses approximated as

$$P_{LOSS} = C_{g'} V_{DD}^2 / T_s + C_{LOAD}(V_{DD} - V_{REF})^2 / T_1 \tag{6.1}$$

$C_{g'}$ is the gate capacitance of surplus power transistors than required by the load and T_s refers to the gate driver rise-time. C_{LOAD} is the load capacitance on the regulated voltage. T_1 is the time difference when regulated voltage reaches its peak value and when it is equal to the reference voltage. Assuming a capacitive load, T_1 is inversely proportional to load current. Similarly, effective $C_{g'}$ increases as load current decreases. Therefore, the power overhead incurred in the digital LDO operation increases if a small load step triggers the non-linear control action. To prevent unnecessary dynamic power loss, the

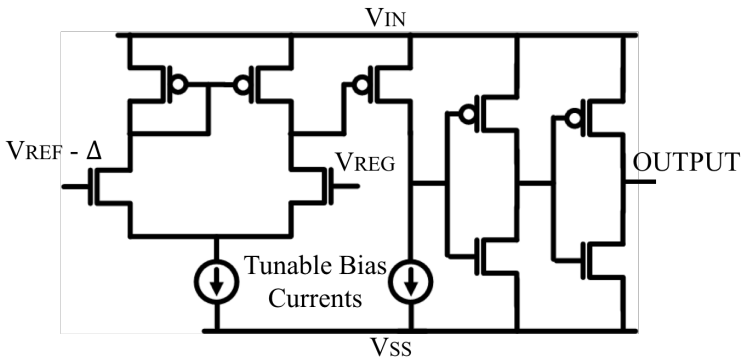


Figure 6.2: Design of asynchronous continuous-time comparator.

voltage droop detection threshold must be placed to account for only large load current transients. To guarantee a stable voltage settling after a non-linear control action and the subsequent voltage overshoot, a low frequency master clock must be employed to allow the regulated voltage to return smoothly to reference voltage without any oscillations.

6.2 Architecture and Design

The basic digital LDO structure is based on the design presented in [12] and explained in earlier chapters as shown in fig. 6.1. This design offers a simple shift register based control logic which is readily synthesizable as a digital circuit. A sense amplifier based comparator detects the difference between V_{REG} and V_{REF}. If $V_{REG} > V_{REF}$, a single power transistor is turned off by using right shift of all the values in the shift register and if $V_{REG} < V_{REF}$, left shift of all the values is performed. In the current implementation, the power stage comprises of 128 equally sized power MOSFETs controlled through 128-bit shift register. The sense amplifier operates on the positive clock edge followed by shift register action on the following clock edge. This dual edge logic reduces the latency between sampling and actuation of the power stage.

Voltage droop detection is performed using a continuous-time comparator comprising of a two-stage amplifier followed by fast slew rate inverters as shown in fig. 6.2. The first stage of the amplifier is an active-loaded differential amplifier. Common-source amplifier

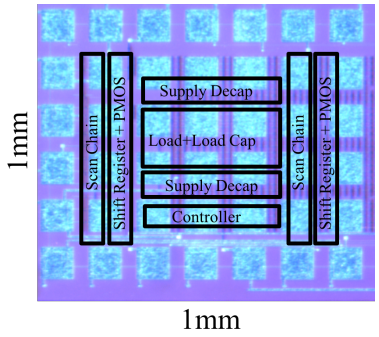


Figure 6.3: Chip micrograph with circuit placement details. The testing is performed on a QFN packaged die.

based second stage is used to enhance the gain of the comparator. The two-stage amplifier is followed by fast slew rate inverters to increase the driving capability and decrease the latency of the comparator action. The tail current of both the stages of two-stage amplifier is externally tunable to allow offset and mismatch compensation. The comparator compares V_{REF}-Δ with V_{REG} to determine the voltage droop. In case of a voltage droop, the output of the comparator is propagated as a reset signal to all of the 128 bits of the shift register flip-flops. This action enables all the power transistors resulting in maximum possible voltage droop mitigation. The comparator topology is kept simple to allow fast decision at minimum possible quiescent current and design overhead.

6.3 Measurement Results

The design is fabricated in 65nm CMOS process. The chip micrograph is shown in fig. 6.3. The nominal supply voltage for high performance mode is 1.2 V. The LDO is designed to deliver a maximum load current of 125mA at a dropout voltage of 600mV occupying a total area of only 0.061mm^2 excluding decoupling capacitor area.

Fig. 6.4 shows the shmoo plot showing the operational range of the designed LDO. Given the simplistic low overhead design of the digital LDO, it can operate with a supply voltage from 0.55V to 1.2V. The regulated output voltage ranges from 0.15V all the way up to 1.15V with a minimum operation dropout voltage of only 50mV. To the best

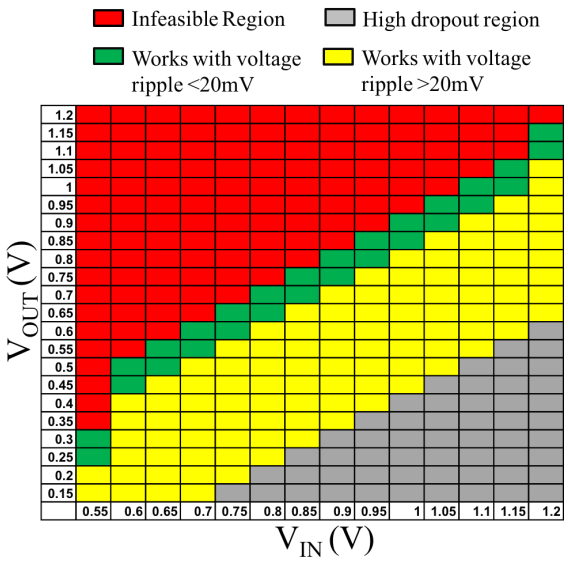


Figure 6.4: Shmoo plot showing the wide operational range of the proposed digital LDO. Load current is not constant at different V_{IN} and V_{OUT}.

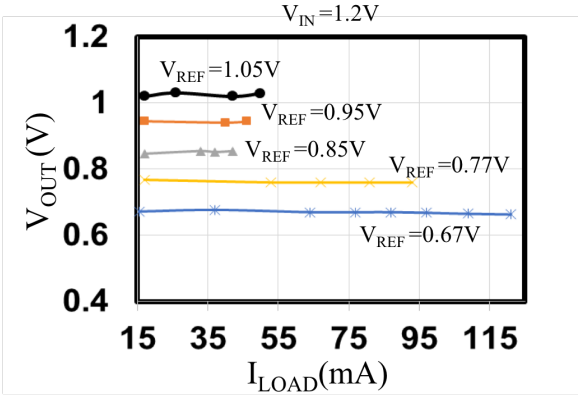


Figure 6.5: Measured Load Regulation.

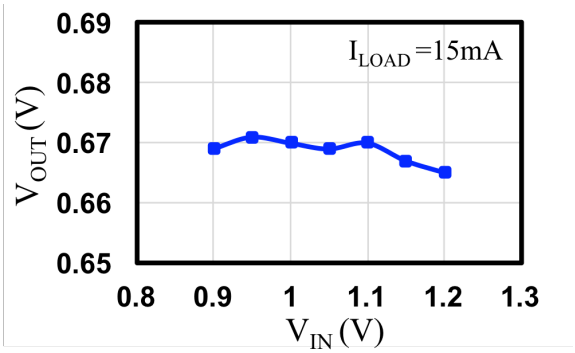
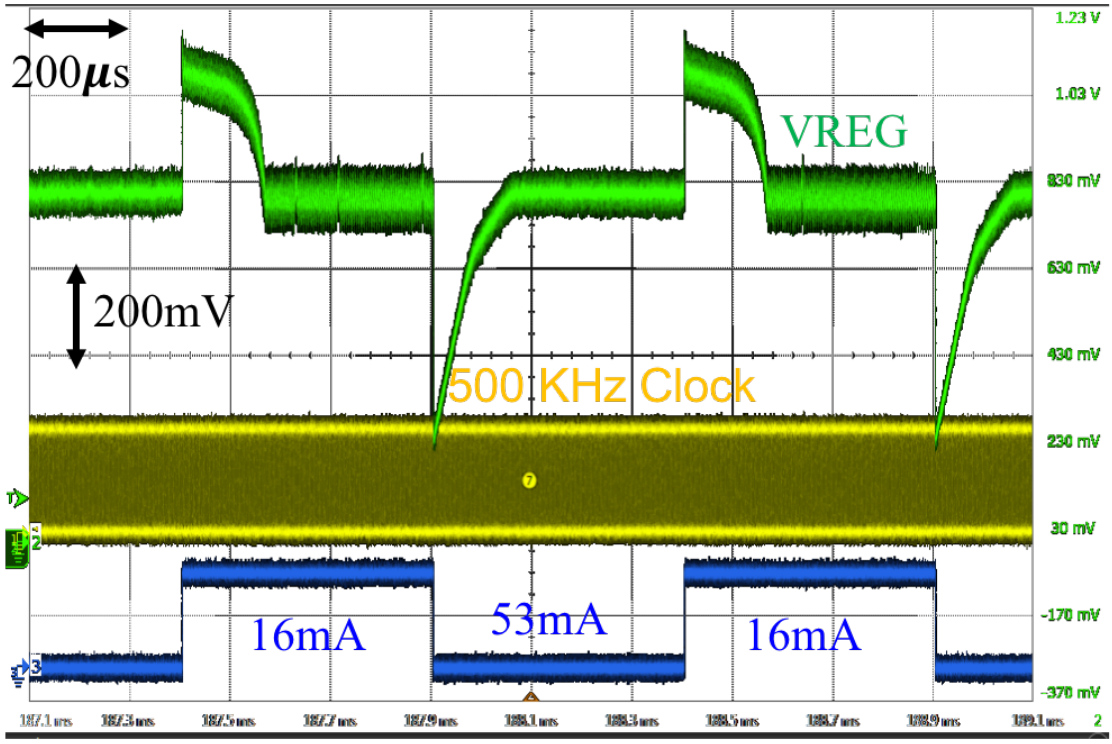


Figure 6.6: Measured Line Regulation with V_{REF}=670mV.

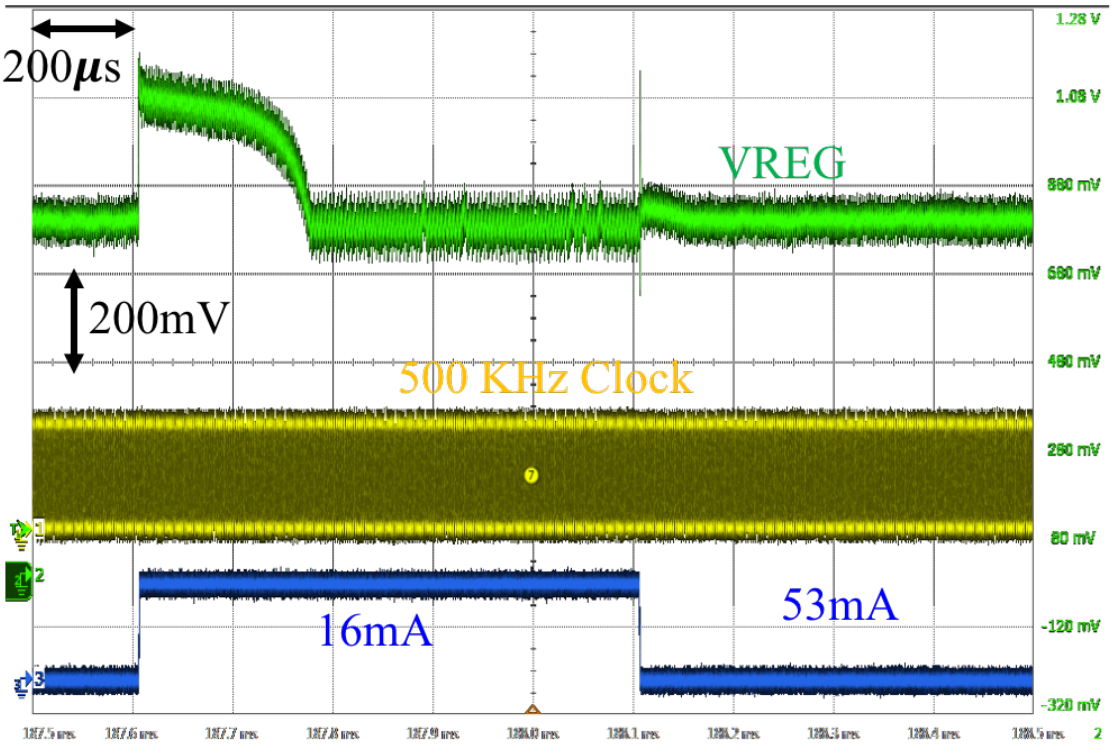
of my knowledge, 0.15V is the lowest regulated voltage reported in the literature. For a dropout voltage of greater than 100mV, the steady-state voltage ripple of the design cannot be guaranteed to be less than 20mV. This is because at an increased dropout voltage, the current contribution of each power transistor grows non-linearly resulting in a larger ripple especially under light load current conditions. Advanced steady-state ripple mitigation techniques like clock adaptation [12] and multiple size power stage quantization [56, 48, 57, 58] can be readily added to this design but are not discussed given the focus of this chapter is on the transient performance.

Load regulation measurements for different dropout voltages are covered in fig. 6.5. The straight-line behavior of the curves across different dropout voltages show that load regulation remains constant across a large current range of 15mA to 121mA. Fig. 6.6 shows line regulation measurements for reference voltage of 670 mV and load current of 15mA when supply voltage varies from 0.9 to 1.2 V. A worst case error of 5mV is measured at the largest dropout voltage.

A comparison of asynchronous non-linear control digital LDO transient performance against a baseline digital only LDO is shown in the oscilloscope captures of fig. 6.7 The voltage droop reduces by almost 425mV as compared to the baseline design for a load step of 16 to 53mA in 1μs transition time with C_{LOAD}=1nF, C_{IN}=2nF and V_{REF}-Δ=750mV. The clock is maintained at a low frequency of only 500 KHz showing almost optimal settling



(a)



(b)

Figure 6.7: Transient plot showing load step and release for (a) baseline digital LDO (b) proposed digital LDO. V_{REF}=875mV, V_{REF}-Δ=750mV.

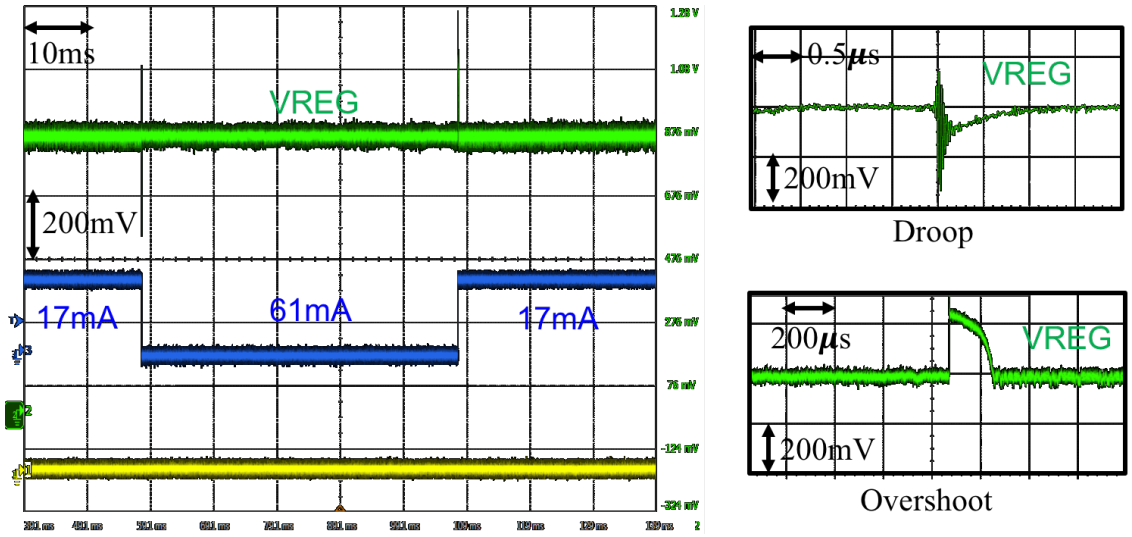


Figure 6.8: Transient performance against large load current step and release with asynchronous non-linear control. V_{REF}=875mV, V_{REF}-Δ=750mV.

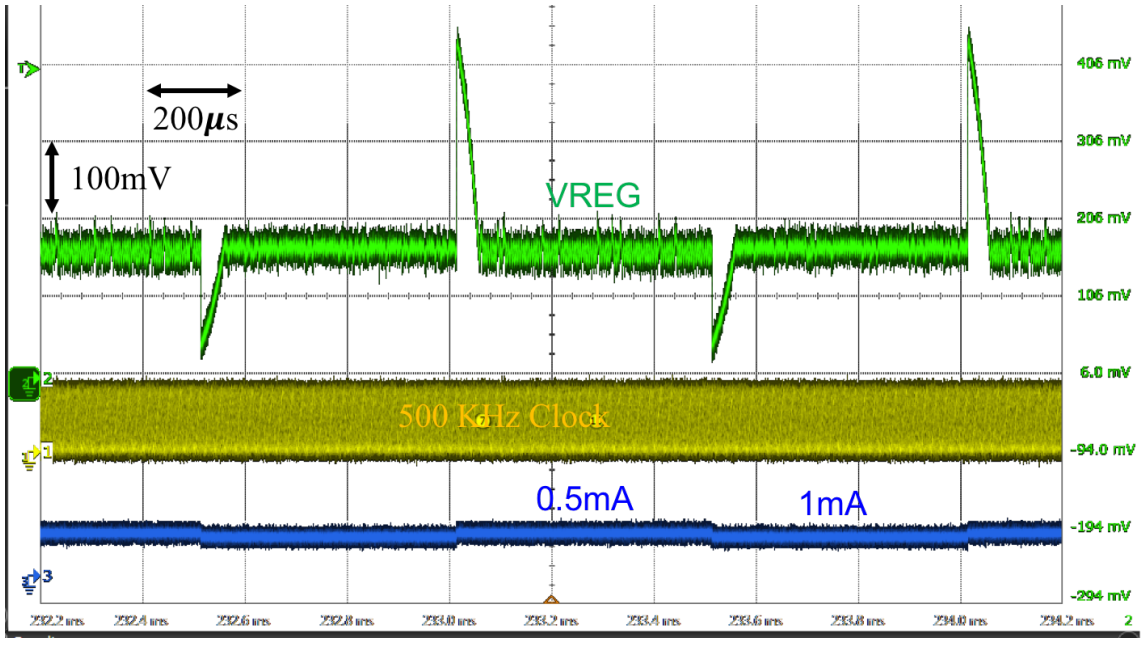


Figure 6.9: Transient performance of baseline digital LDO at V_{REF}=150mV and V_{IN}=1.2V.

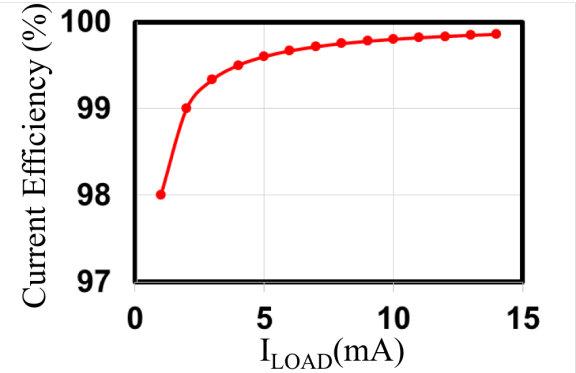


Figure 6.10: Measured static current efficiency of the proposed design.

Table 6.1: Comparison Table

	This work	[56]	[48]	[57]	[58]
Type	DLDO with async. non-linear droop mitigation	Async. DLDO	DLDO	DLDO	DLDO
Process (nm)	65	65	40	28	65
V_{IN} (V)	0.55-1.2	0.6-1	0.6-1.1	1.1	0.6-1.1
V_{REG} (V)	0.15-1.15	0.55-0.95	0.5-1	0.9	0.4-1
$I_{LOAD,MAX}$ (mA)	125	500	210	200	100
F_{CLOCK} (MHz)	0.5	-	N/A	N/A	500
C_{LOAD} (nF)	1	1.5	20	23.5	1
C_{IN} (nF)	1-1000	N/A	N/A	N/A	N/A
I_Q (uA)	0-20	300	22.6-98.5	110	82
Load Reg. (V/A)	<0.18	0.25	0.075	N/A	0.06
Area (mm^2)	0.061	0.158	0.192	0.021	0.01
Max Curr. Efficiency (%)	99.99	99.99	99.99	99.94	99.92

after non-linearly recovering from a voltage droop. To account for varying decoupling capacitor budget and load transition rates, as expected in a digital load circuit, the supply capacitance is increased to 1μF and load step transition edge is reduced to only 2ns. Under such a scenario, a voltage droop of approximately 350mV is measured for load step of 44mA as shown in fig. 6.8. Package and board resonances due to parasitic package inductance contributes to the oscillatory behavior before the voltage settles. These second order effects are not observed for digital LDOs targeting a small current range of a few mA and proves that the PDN must be designed carefully. Low regulated voltage operation of the proposed LDO is measured at a regulated voltage of 0.15V under a load step 0.5mA, as shown in fig. 6.9. At low voltage operation, the droop comparator is non-operational and only the digital LDO is used.

A measured quiescent current of only 20μA, mostly consumed by the droop detection comparator, allows a measured current efficiency of greater than 99.5% for just 4mA load current as shown in in fig. 6.10. A comparison with current state-of-the-art designs show competitive performance of the proposed LDO as summarized in Table 6.1.

CHAPTER 7
OVERCOMING LIMITATIONS OF DIGITAL LDO WITH ANALOG ASSISTANCE

In previous chapters, the effectiveness of digital LDOs in powering wide dynamic range digital load circuits was established. The insights derived from theoretical modeling of the digital LDOs were supported with experimental verification through test-chips. In this chapter, the author has tried to establish the motivation of pursuing research on hybrid LDOs using insights obtained through a test-chip.

A digital LDO is more readily synthesizable in a digital process flow as compared to its analog counterpart. It boasts the ability to easily adapt its transient performance based on the load requirement making it an attractive solution for digital load circuits with wide operational ranges. Similarly, these adaptation knobs can also be tuned to save power in low power/sleep states, which makes digital LDOs suitable for low power Internet-of-Things (IoT) applications. Where digital LDOs offer many advantages, they also suffer from few limitations. The two prime shortcomings are limited steady-state voltage regulation accuracy and low power supply noise rejection (PSR).

To enable widespread use of digital LDOs for on-chip voltage regulation of all types of load circuits and not just digital load circuits, these limitations must be addressed. To this end, we present a hybrid LDO macro as shown in fig. 7.1. It combines in parallel fashion the discrete feedback control mechanism of a digital LDO with the continuous feedback obtained through an analog LDO. The proposed design helps in minimizing the steady state limit cycle oscillations. The design is validated with a 130 nm test chip and measurement results have been provided to show the efficacy and limitations of the proposed hybrid LDO topology.

The trade-offs involved in the design of a digital LDOs are now well understood thanks

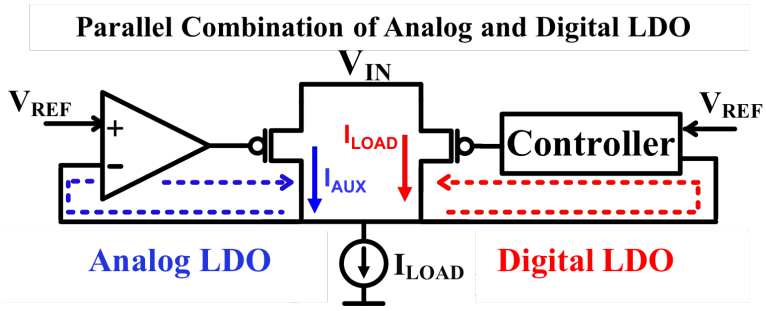


Figure 7.1: Proposed hybrid LDO topology.

to the aforementioned research explained in this thesis. We understand that there exists an inherent trade-off between the transient and steady-state performance of digital LDOs. To satisfy ultra-fast transient performance requirement of digital load circuits, there is a need to push the F_S in the GHz region. This action increase the steady-state limit cycle oscillations of a digital LDO as shown in the test-chip scope capture of a 16-bit digital LDO in fig. 7.2. To achieve a better steady-state performance, mode of steady-state limit cycle oscillations has to be contained at high F_S. Two solutions have been proposed in the recent past to achieve this goal. First is the use of a dead-zone around the regulation voltage as discussed in chapter 4. It results in no output ripple, but limits the DC accuracy of the LDO. Second solution uses a feed-forward path based compensation [59]. It requires feed-forward path gain calibration to be applicable across a wide range of F_S. In this chapter, we present an analog assisted digital LDO, which limits the mode across a wider range of F_S. The proposed hybrid LDO macro is elaborated in section 1 with a discussion on the proposed topology in section 2.

7.1 Hybrid LDO

The oscillatory discrete dynamics of the digital LDO are aided with continuous dynamics of an analog LDO to compensate the instantaneous small signal variations and reduce the mode of limit cycle oscillations. The proposed design covered in this chapter provides mode reduction across a load current range of 153μA to 1.7mA for an F_S ranging from 2

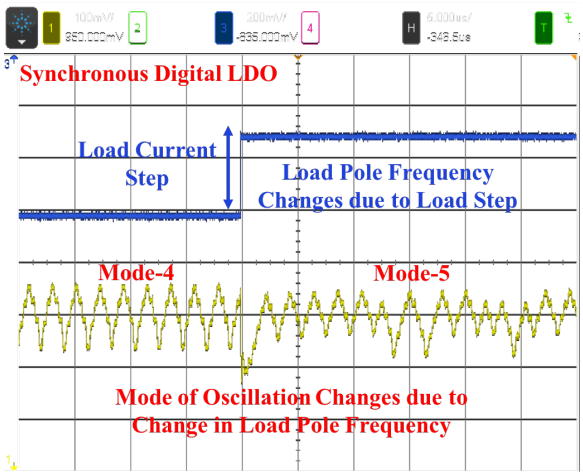


Figure 7.2: Measured verification of limit cycle oscillations in digital LDO.

to 30MHz.

7.1.1 Stability

The digital LDO is assisted with a parallel analog LDO to suppress steady state limit cycle oscillations. Stability of the parallel combination of a digital and an analog LDO is guaranteed by designing an output pole dominant analog LDO. This analog LDO remains stable under the complete load current range of the hybrid topology. Ensuring stability with a hybrid combination of a digital LDO and an internal pole dominant LDO is more difficult. Since the dominant pole of a digital LDO is at the output, the phase margin of the overall system will reduce when another dominant pole is located at another node (internal node of the analog LDO). Similarly, any imbalance in current or uneven load sharing may also excite the light load instability condition of an internal pole dominant analog LDO.

7.1.2 Circuit Implementation

The proposed digital LDO is a synchronous digital LDO capable of providing up to 3mA of load current. The design of digital LDO explained in chapter 3 is followed here. It has a strong-ARM latch based clocked comparator followed by a 16-bit shift register and an output array of 16 power MOSFETs. The output pole dominant analog LDO is capable

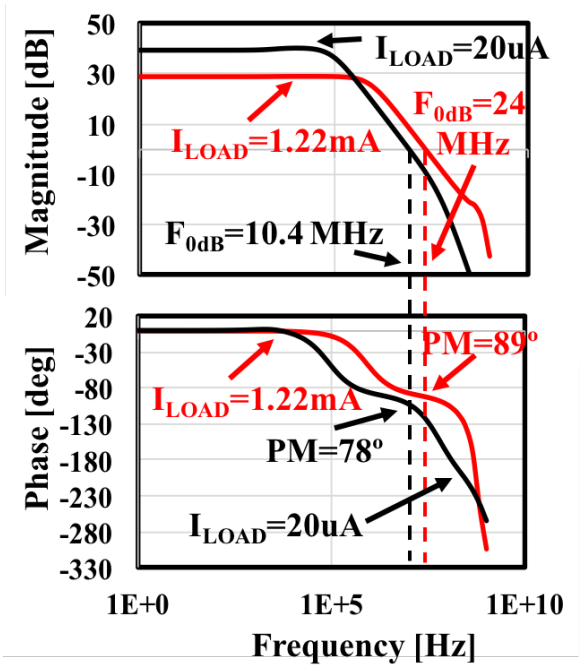


Figure 7.3: Bode plot of output pole dominant analog LDO.

of providing up to 1.25mA of load current. The exact design of the LDO is covered in next chapter. The test-chip has two replicas, which can supply up to 2.5mA load current. A simulated gain of 29dB and 39dB is achieved when the load current is 1.25mA and 20μA, respectively. The bandwidth of the analog LDO changes (increases) with changing (increases) load current and under maximum load current conditions, each replica has a PM greater than 85° as shown in fig. 7.3. The designed analog LDO has two stages. The first stage is an operational transconductance amplifier. It is followed by a shunt feedback stage and a power MOSFET. The shunt feedback stage converts the internal pole at the gate of the power MOSFET in to two high frequency poles, thereby, achieving an output pole dominant analog LDO. The design has a total on-die capacitance of less than 500pF at the output.

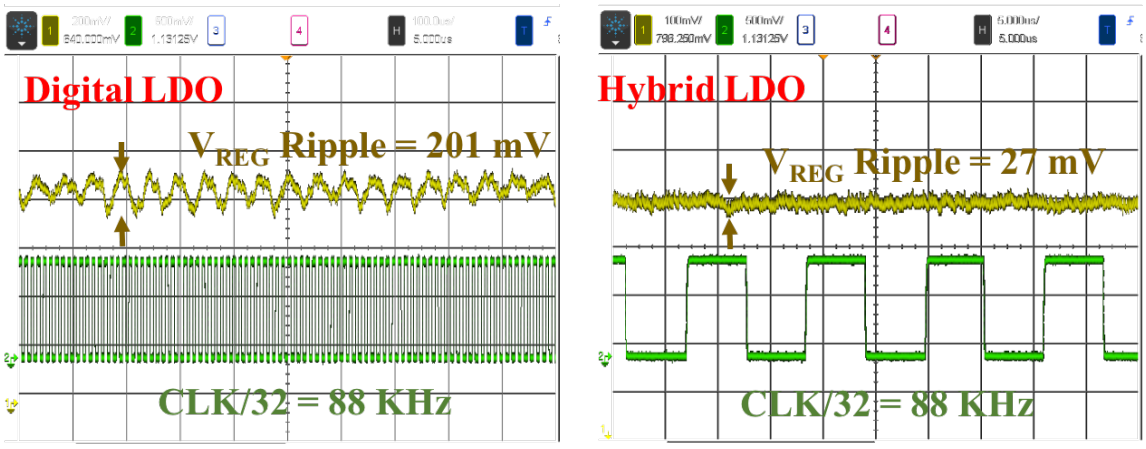


Figure 7.4: Measured reduction in output ripple with hybrid topology.

7.1.3 Mode Reduction

Due to the bang-bang control nature of the digital LDO, load current is always varying. With increasing mode at a higher F_S, this variation becomes larger and results in larger ripple. The analog LDO limits this ripple by compensating for the difference between the current provided by the digital LDO and required by the load circuit, as shown by the scope capture in fig. 7.4. A higher gain-bandwidth product ensures better mode reduction. With analog assistance, the mode reduction can be observed throughout the operational F_S of 2MHz to 30MHz, as shown by the simulated results of fig. 7.5. As elaborated in chapter 4, the exact output ripple amplitude is a function of the size of power MOSFETs. An increase in mode increases the output ripple but if the mode remains same for increasing F_S, the ripple goes down. The reduction in the ripple through the use of the hybrid topology can be clearly observed when it is compared to a digital only solution. The decrease in the output ripple at iso-F_S is representative of decreased mode when analog LDO is enabled. Increasing the size of analog LDO power MOSFET by 2x, strengthens its performance parameters (gain, BW and slew rate) and further decreases mode-2 to a mode-1 oscillation at F_S=30 MHz for I_{LOAD}=1.7mA (not shown in the figure).

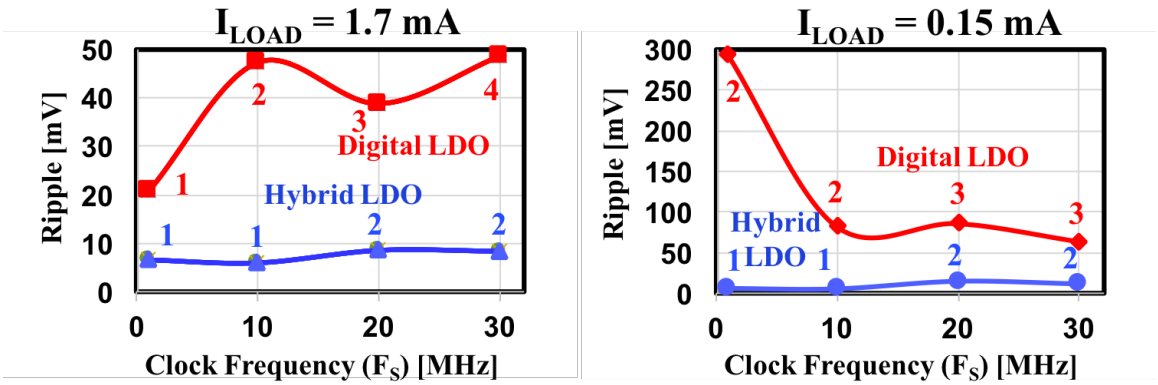


Figure 7.5: Simulated reduction of mode (shown in numbers) of limit cycle oscillations at I_{LOAD}=1.7mA and I_{LOAD}=153μA with hybrid as compared to a digital LDO.

7.2 Discussion on the Hybrid Topology

Continuous time dynamics of an analog LDO aids in reducing the steady state limit cycle oscillations inherent to the operation of digital LDOs. With increasing F_S, the transient performance of the digital LDO improves. To keep a consistent mode reduction, the gain-bandwidth and slew rate of the analog LDO must be increased as well. If this adaptation is not performed, an unequal current distribution makes one loop stronger than the other and all the benefits of the parallel hybrid topology are lost. This is illustrated with simulation results of fig. 7.6. The strength of the digital LDO is increased by increasing the size of the output power MOSFETs while the analog LDO strength is kept same. It can be clearly seen that the mode decreases in hybrid topology but the improvement is not uniform because of the uneven load current sharing and controller strengths. Unless, the specifications are not defined in terms of worst case bounds, ensuring uniform performance across the complete range of operation is difficult. Furthermore, with increasing process, voltage and temperature variations, ensuring the utility of the hybrid topology in parallel combination becomes even more difficult. To realize hybrid LDOs with operational frequencies reaching GHz, a large amount of power has to be consumed in the analog LDO to guarantee performance improvement. Otherwise, one of the controllers will overpower the other one. Although the

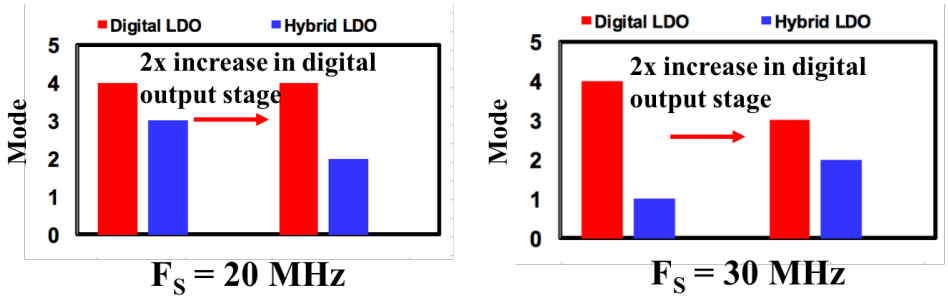


Figure 7.6: Simulated reduction in mode of digital LDO with hybrid topology at F_S=20MHz and F_S=30MHz for iso-biasing of the analog LDO.

combination of discrete with continuous dynamics is a powerful paradigm to cater for wide dynamic range of digital load circuits but better control topologies are required to harness its full performance. One such topology based on switched-mode-control is presented in the next chapter.

CHAPTER 8

SWITCHED-MODE-CONTROL BASED HYBRID LINEAR VOLTAGE REGULATOR

Building on the insights of chapter 7 to devise better control topologies of hybrid LDO, a new control topology for LDOs namely, switched mode control (SMC) is covered in this chapter. Through a test-chip built in 130nm CMOS, its efficacy in designing low-power and fast LDOs covering a wide operational range for all types of load circuits is emphasized.

PoL voltage regulation of digital load circuits needs to satisfy a different set of constraints than that offered by traditional analog load circuits [4]. For example, digital circuits can withstand a lower power supply noise rejection, but require fast transient recovery under large voltage droops and operation down to Near-Threshold-Voltage (NTV) with minimum dropout. To meet these challenges, both analog and digital LDOs are being researched; and they have their own strengths and weaknesses. Analog LDOs exhibit accurate small signal (SS) regulation, but lack voltage and process scalability and the ability to handle large current transients [34, 35]. On the other hand, digital LDOs are characterized by fast large signal (LS) performance but they lack high SS gain. They also show steady state ripple and consume clocking and dynamic power.

In this chapter, Switched Mode Control (SMC) is proposed which combines controllers optimized for different metrics to increase operational range and performance without compromising the overall stability. A high-performance SMC based hybrid LDO designed in a 130nm CMOS process is presented. The proposed design decouples the SS gain from LS transient response by utilizing a voltage based error signal to discretely switch from one controller to another. This is fundamentally different from other dual loop architectures [34, 42, 14], which employ both the loops simultaneously. In such designs, the bandwidth of high-gain loop is decreased to maintain stability (fig. 8.1a). The hybrid LDO uses SMC

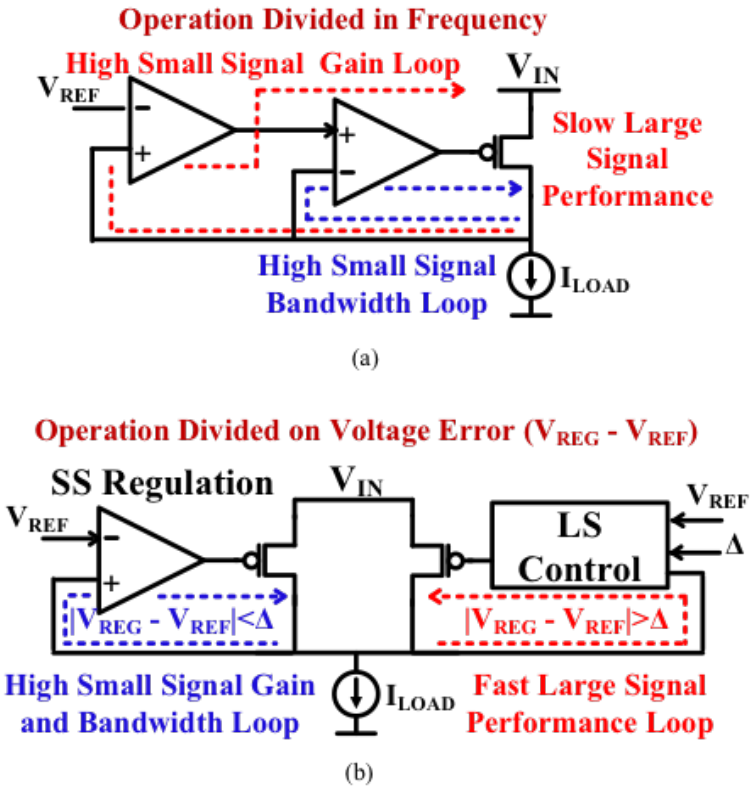


Figure 8.1: (a) Conventional dual loop LDOs (b) SMC based multiple controller LDO design.

to combine the strengths of both analog and digital LDOs. It combines the LS response (transient performance) of an all-digital loop, with the high-gain steady state voltage regulation offered by an analog loop (see fig. 8.1b), thus enabling optimal control across a wide operating range. The addition of analog assistance to the digital loop enables a high-performance hybrid LDO operation at higher power supply voltages ranging from 1.2 to 1.1 V. To provide voltage regulation at low power supply voltage down to 0.6V and still ensure process and design scalability, SMC further enables the hybrid LDO to be turned into an all-digital LDO without compromising design stability or consuming additional power.

The need for using SMC instead of a single controller is motivated in Section 1. In Section 2, the hybrid LDO architecture is elaborated. Stability modeling of SMC and an ultra-fast response time design feature called SMC with reset control are presented in Section 3 and 4, respectively. Circuit implementation of the hybrid LDO is covered in

Section 5. Measurement results from the test-chip are covered in Section 6.

8.1 Motivation for Switched Mode Control

Since digital load circuits exhibit large load current (I_{LOAD}) changes and operate under wide operational voltage ranges (from V_{MAX} to NTV), it is difficult to ensure fast transient response using a single controller across the entire current and voltage range [14]. For example, an analog LDO provides high performance at near-supply input voltage but fails at NTV [34] and a digital LDO offers low voltage operation but shows a reduced power efficiency if operated in high performance mode [12]. Therefore, the motivation for SMC stems from the fact that multiple controllers extend the operational range at a better power efficiency.

The step response of a second order linear system determines all the critical parameters that are needed to ascertain the effectiveness of the feedback. A fast rise time ensures quick recovery from a transient event. A fast and accurate settling ensures accurate tracking of a reference voltage (V_{REF}). On the other hand, a minimum overshoot reduces unwanted ringing. These three factors can be combined into a quantitative cost metric, which characterizes the typical feedback control of an LDO, defined in [60] as:

$$Cost = \int_0^\infty t|V_{REF} - V_{REG}|dt \tag{8.1}$$

The cost defined above, is the minimum integral of time-multiplied absolute-value of error. It shows a high sensitivity to the three discussed parameters crucial to any second order system dynamics. The cost increases if the rise time is slow or settling takes longer or the response shows large overshoot or undershoot. In linear voltage regulation, optimal criterion for LS region is fast rise time (T_{RISE}). For SS region, it is fast settling time ($T_{SETTLING}$) with minimum overshoot. SMC allows the two separate optimal controllers to be combined by switching at a threshold to achieve an overall optimal response to LS

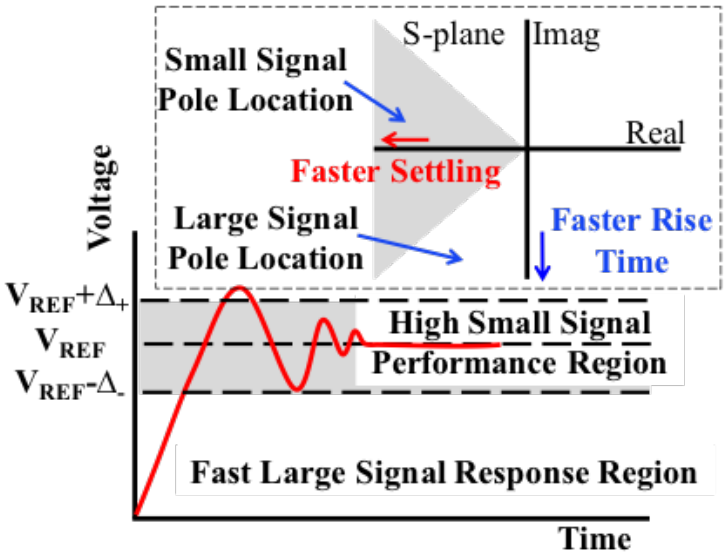


Figure 8.2: Ideal closed loop pole locations for large signal and small signal controllers.

current transients. Location of the dominant pole of the overall system for each controller determines its response as illustrated in fig. 8.2. For a fast LS response, the dominant poles of the system should have a low damping which enables a small T_{RISE}. On the other hand, a short $T_{SETTLING}$ is achieved by placing the dominant poles of the system deep in the left half s-plane. It can be clearly seen that an SMC based on the combination of an underdamped and overdamped controllers outperforms both individually in terms of the cost metric defined in (8.1) as shown through the step response of different systems in fig. 8.3.

8.2 Hybrid LDO Design Architecture

8.2.1 Choice of SS and LS Controllers

Choosing optimal controllers for each region of operation ensures optimal performance across the complete current and voltage operational range. As summarized in Table 8.1, a higher integration density, process scalability, design automation, low voltage operation and most importantly, ultra-fast response without slew limitation, makes digital LDO an ideal choice to act as the LS controller. It allows faster recovery from load transients and

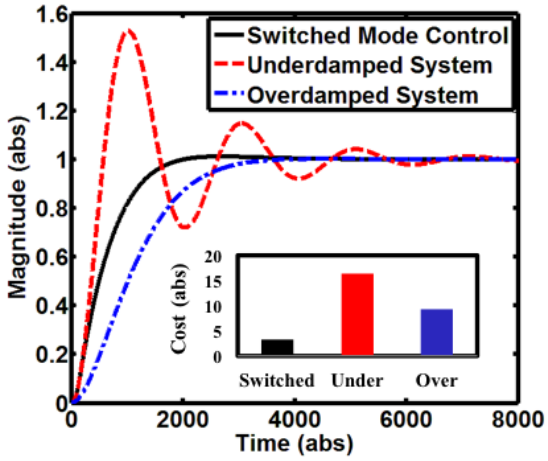


Figure 8.3: Effectiveness of SMC compared to a single controller design.

Table 8.1: Selection of LS controller topology.

LS LDO Topology Characterization		
Type of LDO	Analog	Digital
Rise Time	Slow	Fast
Small Signal Gain	High	Low
Process Scalability	Low	High
Design Automation	Low	High
Performance Adaptation	Low	High
Design Choice		✔

Table 8.2: Selection of SS controller topology.

SS Analog LDO Topology Characterization		
Dominant Pole Location	Internal	Output
V_{DROOP}	High	Low
PSR over all frequency	Low	High
UGF	Low	High
Light Load Stability	Poor	Good
On chip Integration	Standard	Difficult
Design Choice		✔

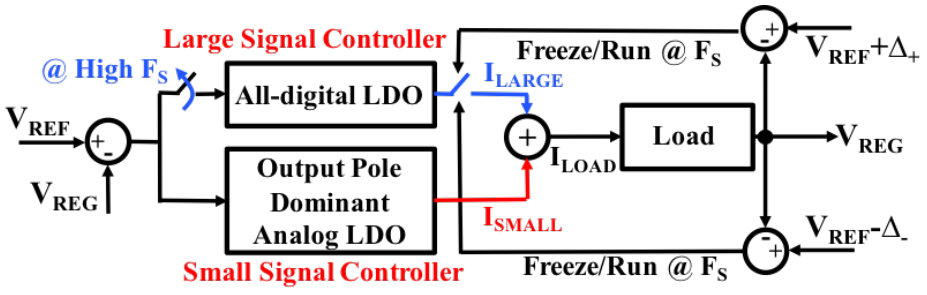


Figure 8.4: Control schematic elaborating switching between different controllers based on the voltage error for the proposed hybrid LDO.

offers wider operating voltages. In addition to that, a digital LDO can be adaptively made severely underdamped with a fast clock as desired for the LS controller following RDS. For SS controller, a small quiescent power consumption, high SS gain, and ripple-free SS response makes analog LDO the design choice. Analog LDOs can be further divided in to two major categories (Table 8.2), Internal pole dominant (IPD) and Output pole dominant (OPD) LDOs. OPD analog LDOs offer better power supply noise rejection, faster droop compensation, and light load stability compared to their IPD counterparts [34]. Therefore, the SS controller design choice should be an OPD analog LDO. It should be mentioned here that a high resolution digital LDO is ill-suited to be used as an SS regulator as it suffers from limit cycle oscillations and limited gain unless high dynamic power budget and clock routing resources are available. Conventionally, a small on-die capacitance budget limits its use in PoL voltage regulation as an OPD analog LDO loses its phase margin (PM) with increasing I_{LOAD} for a given output capacitance. The presented hybrid topology overcomes this integration challenge by using LS controller to deliver most of I_{LOAD}, relaxing the constraints on the SS controller design.

8.2.2 Hybrid LDO Operation

The digital LS controller turns on a power transistor array in a thermometer fashion until V_{REG} reaches $V_{REF} - \Delta_-$. Once V_{REG} enters the dead-zone, LS controller is clock-gated and the SS controller provides the remaining I_{LOAD} bringing V_{REG} to V_{REF}. For an over-

shoot, $V_{REG} + \Delta_+$ acts as the dead-zone boundary with SS controller operational when $V_{REG} < V_{REF} + \Delta_+$. The LS digital controller power transistors are designed to provide 80-90% of the I_{LOAD} whereas the SS analog controller provides the remaining 10-20% of I_{LOAD} at the maximum current rating. This range is ensured keeping in perspective that an increased I_{LOAD} contribution from the analog LDO diminishes the performance gains of an all-digital LDO as elaborated in [61]. The high operational bandwidth of the LS controller makes SS controller ineffective when it is active and V_{REG} is out of the dead-zone. Therefore, there is no need to explicitly turn off the SS controller when $V_{REF} - V_{REG} > |\Delta|$. This also helps in eradicating switching noise and power overhead of explicitly switching SS analog controller on or off. The dead-zone helps bound the limit cycle oscillations (LCO) in digital LS controller when it is operated at a high frequency of operation increasing the stability of the hybrid LDO. The choice of switching thresholds not only achieves stable operation (no chattering between the two controllers) but also ensures that the analog LDO only provides a small portion of the total I_{LOAD} (10-20%), thereby assisting the dominant digital operation of the hybrid LDO through an output pole dominant analog LDO design. The switching between the two controllers is summarized through the control schematic shown in fig. 8.4 and a complete system architecture of the proposed hybrid LDO is shown in fig. 8.5 with operational plots in fig. 8.6(a,b,c). Digital load circuits are mimicked by NMOS transistors. Their strength is scan programmable allowing both transient and steady state current changes on the order of ps. A 500pF (at 1V) MOS capacitor serves as the load capacitor to mimic a realistic capacitance offered by a medium-sized digital load circuit [41].

8.3 Stability Modeling

To stitch a fast and underdamped LS digital controller to a slow and damped SS analog controller in a stable fashion, a dead-zone is established using two thresholds above and below V_{REF}. The digital LS controller creates limit cycle oscillations (LCO) due to its discrete na-

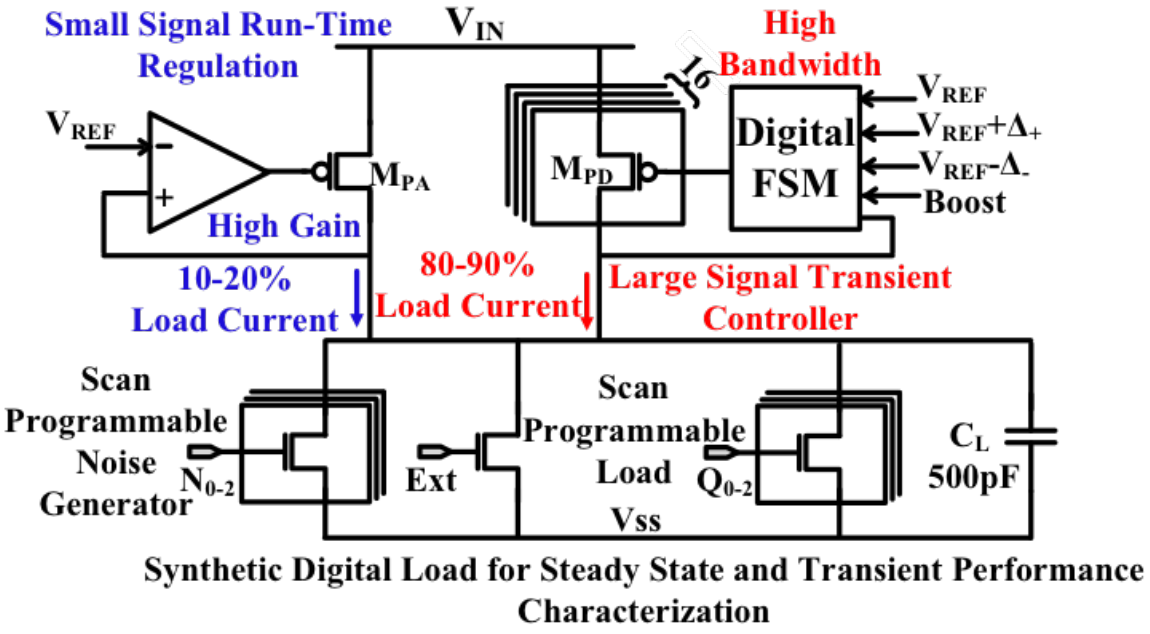


Figure 8.5: SMC based Hybrid LDO architecture with load.

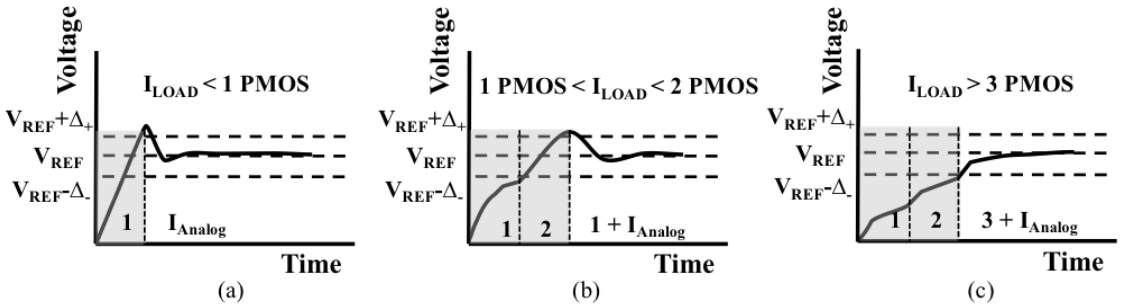


Figure 8.6: Operation of hybrid LDO with increasing I_{LOAD} (a) I_{LOAD} supplied by SS controller only (b,c) I_{LOAD} supplied by both LS and SS controllers (LS clock frequency $\sim$ output pole frequency).

ture of operation. These LCO are created by periodically turning on/off power transistors. The number of power transistors turned-on/off in steady state is called mode. The mode of LCO increases with higher F_S. As a result, the V_{REG} voltage ripple frequency ($F_{LCO,LS}$) decreases. On the other hand, the V_{REG} voltage ripple amplitude ($A_{LCO,LS}$) decreases when F_S increases but shows a jump rise whenever, the mode of LCO increases. For more details on the existence, conditions and magnitude of LCO, interested readers are pointed to chapters 3 and 4 for further reading. For stable and chattering-less settling to V_{REF}, the SS controllers must have enough loop-gain (K_{SS}) and bandwidth ($F_{0dB,SS}$) to suppress the oscillations generated by the digital LS controller. Stable operation of the hybrid LDO can be achieved by satisfying the following design constraints.

Bandwidth Constraint:

$$A_{LCO,LS} > (V_{REF} + \Delta_+ - V_{REF} + \Delta_-); F_{0dB,SS} > F_{LCO,LS}; \tag{8.2}$$

Amplitude Constraint:

$$F_{0dB,SS} < F_{LCO,LS}; A_{LCO,LS} < (V_{REF} + \Delta_+ - V_{REF} + \Delta_-); \tag{8.3}$$

Small Signal Constraint:

$$V_{REF} - \Delta_- < (V_{REF} - \frac{V_{REF}}{1 + K_{SS}} < V_{REF} + \Delta_+; \tag{8.4}$$

$A_{LCO,LS}$ and $F_{LCO,LS}$ refer to the voltage ripple amplitude and frequency of the LCO generated by the LS controller if it is operated without any dead-zone and SS controller. The bandwidth constraint in (8.2) implies that if the dead-zone is small compared to the LS controller power transistors quantization then we need $F_{0dB,SS}$ higher than $F_{LCO,LS}$ to ensure stable settling. On the other hand, the amplitude constraint in (8.3) implies that if the $F_{0dB,SS}$ is less than $F_{LCO,LS}$ then $A_{LCO,LS}$ must be less than the dead-zone to ensure stable settling.

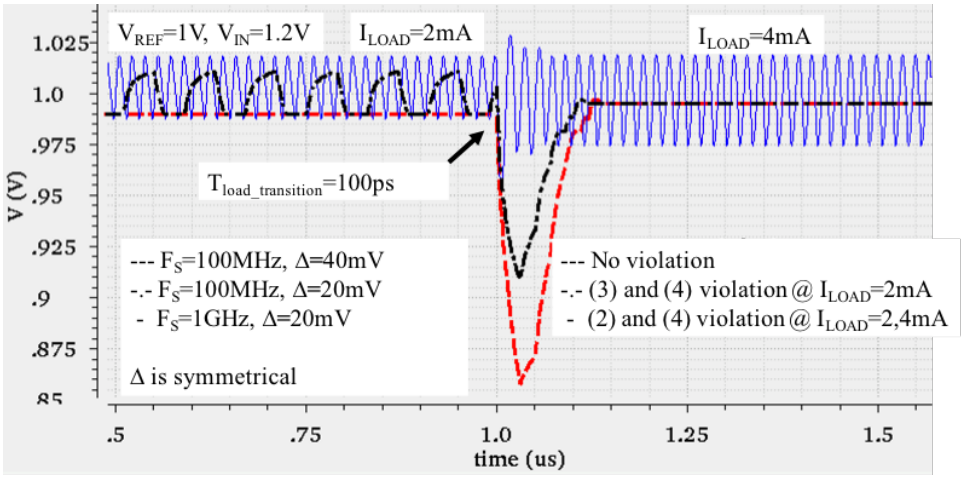


Figure 8.7: SPICE simulation of the hybrid LDO showing conditions where stability constraints are violated resulting in an unstable behavior.

The small signal gain constraint in (8.4) implies that K_{SS} must be large enough to ensure that the steady state voltage error is less than the dead-zone size to avoid chattering between LS and SS controllers. One of the bandwidth or amplitude constraints and small signal gain constraint must be satisfied to guarantee stable operation of the hybrid LDO. Possible worst case amplitude constraint (8.3) violations occur under light load conditions and frequency constraint (8.2) violations occur at very high operational frequencies as shown in SPICE simulation of fig. 8.7.

A large dead-zone ensures that multiple power transistors of the LS controllers are needed to traverse it. At iso-F_S, it implies a decreased $F_{LCO,LS}$ relaxing the specification on $F_{0dB,SS}$. Similarly, a large dead-zone also relaxes the specification on K_{SS}. If F_{LCO} induced by the LS controller in the dead-zone lies below F_{0dB} of the SS controller, and the dead-zone is large to ensure that $A_{LCO,LS} < (\Delta_+ + \Delta_-)$ then the hybrid LDO is guaranteed to be stable. The exact settling time and accuracy of the output voltage is dependent on the load regulation of the SS controller. A higher F_{0dB} ensures that oscillations in the dead-zone quickly die down resulting in faster settling as shown in fig. 8.8. The voltage settles down to V_{REF} within an error bounded by the loop gain (K_{SS}) of the SS regulator.

Although a large dead-zone enables a more relaxed specification on the bandwidth of

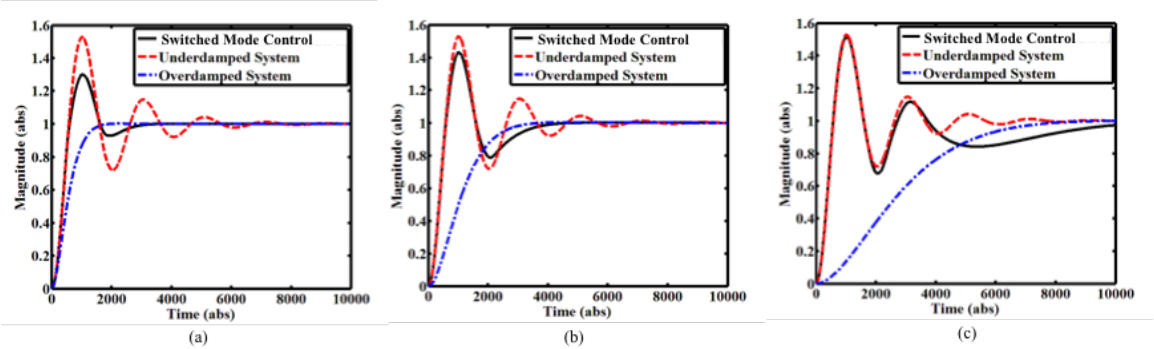


Figure 8.8: Decreasing the bandwidth (BW) of SS controllers increases the settling time ($T_{SETTLING}$) of the SMC design (a) BW(overdamped system)=BW(underdamped system)/3, (b) BW(overdamped system)=BW(underdamped system)/6, (c) BW(overdamped system)=BW(underdamped system)/12.

the SS controller, it may not be suitable for early detection and mitigation of voltage droops and overshoots. More discussion on the selection of thresholds for the hybrid LDO is carried out later with test-chip measurements. As evident from the above discussion, amplitude and bandwidth conditions for a digital LS controller are easy to formulate owing to its discrete nature of operation. This allows well posed constraints for achieving stable hybrid LDO operation. In case the LS controller is analog, similar amplitude and frequency conditions can be devised by identifying the natural frequency and damping coefficient from the closed loop pole location.

8.4 SMC with Reset Control

Synchronous digital circuits are designed with a guard-band to operate as soon as the voltage is high enough (V_{MIN}, where $V_{MIN} = V_{REF}$ - voltage guard-band added to ensure correct operation under variations) to support a target operational frequency (F_{OP}) [23]. Therefore, any voltage higher than V_{MIN} ensures that the underlying circuit can resume operation without any timing errors in the pipeline of digital circuits. For such load circuits, ultra-fast droop recovery to V_{MIN} is necessary for high performance quick resumption of operation. To meet this requirement, we propose a reset mode in the hybrid SMC based LDO similar to the one discussed in chapter 6. This mode enables ultra-fast droop recovery to V_{REF}

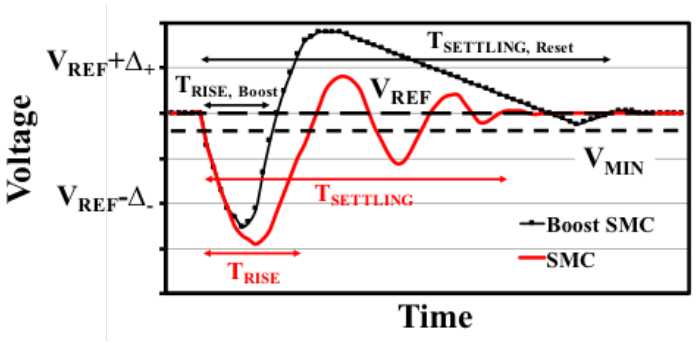


Figure 8.9: Reset SMC shows quicker resumption (equal to T_{RISE}, Reset) of digital load circuit operation (the digital load can achieve operational frequency when $V_{REG}>V_{MIN}$) after a voltage droop as compared to the SMC (equal to $T_{SETTLING}$). V_{REF}-V_{MIN}=Digital load guard-band.

under the condition that the constraints on the overshoot are relaxed. In this extreme non-linear design, as soon as the output voltage reaches $V_{REF} - \Delta_-$ all the power MOSFETs of the digital loop are turned on, enabling ultra-fast T_{RISE}. After recovering from the droop, the system undergoes a large overshoot (always less than V_{IN} as inherent negative feedback of PMOS V_{SD} kicks in against decreasing voltage headroom) and finally settles down to V_{REF} in an overdamped fashion never falling below V_{MIN}. This reset mode SMC is compared with the regular operation of the hybrid LDO in SMC configuration through the representative operational plot shown in fig. 8.9. It shows a faster T_{RISE} ensuring an early resumption of the digital load operation than achievable through the SMC design. This reset mode feature is designed as a part of the digital LS controller. The reset mode is recommended for fast droop recovery under large transient events like clock un-gating and under the assumption that the constraints on the overshoot are relaxed. The reset mode is enabled by the non-linear SMC by allowing the loop dynamics to be completely different in the two regions: quick and underdamped in undershoot and slow and overdamped in overshoot.

8.5 Hybrid LDO Circuit Implementation

8.5.1 Large Signal (LS) Controller Design

A synchronous all-digital LDO with 16 output power transistors is implemented. The small array size with large power transistors as opposed to a larger array size with smaller transistors guarantees a fast LS response [8]. It comprises of four stages, namely, a detection stage to determine the magnitude of the voltage error, a comparison stage to determine the sign of the voltage error, a control stage and an actuator stage. The detection stage consists of two strongARM latch based clocked comparators. They are used to compare V_{REG} with $V_{REF} - \Delta_-$ and $V_{REF} + \Delta_+$ to establish if $V_{REF} - V_{REG} > |\Delta|$. The comparators are designed to operate up to 1 GHz. If V_{REG} is found to be $< V_{REF} - \Delta_-$ or $> V_{REF} + \Delta_+$, i.e., out of the dead-zone, the clock signal is un-gated to the following comparison stage. The comparison stage consists of a single strongARM latch based clocked comparator. It is only operational if the clock is available to it from the preceding detection stage. Once on, it compares V_{REG} with V_{REF}. The control stage consists of a 16-bit bi-directional shift register. If $V_{REG}<V_{REF}$, the shift register passes a logic-0 to turn on a power transistor and if $V_{REG}>V_{REF}$ then it passes a logic-1 to turn off a power transistor, in the final actuator stage. The comparison stage operates at the positive clock edge, whereas, the control stages uses the negative clock edge for its operation. This dual edge triggering allows a lower control signal latency. The final actuator stage consists of an array of 16 power transistors.

In reset mode, all the transistors are instantaneously switched on by resetting the shift register when a droop is detected by $V_{REF} - \Delta_-$ comparator. A regular digital LDO operation is resumed for $V_{REG}>V_{REF}$ at a slower F_S. The power transistor array is designed to provide a maximum current (I_{LOAD}) of 12 mA consuming a total area of 27.68 μm^2. The clock for the LS controller is generated through a five-stage current starved inverter based voltage controlled oscillator (VCO). The bias voltage control of this VCO is available externally on a pad. The oscillator frequency can be tuned up to 1 GHz. A detailed circuit

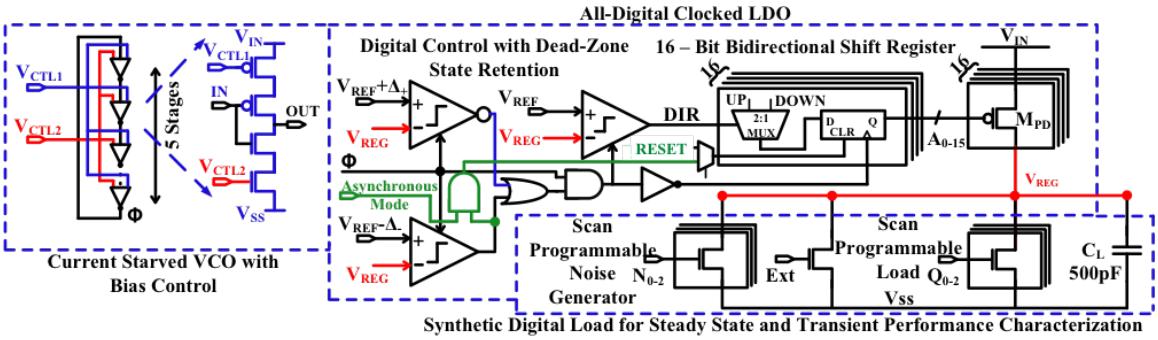


Figure 8.10: Large Signal (LS) controller with clock generation through a 5-stage current starved voltage controlled oscillator. Reset SMC is enabled when Asynchronous mode=1.

implementation of the LS controller along with the current starved VCO is shown in fig. 8.10.

8.5.2 Small Signal (SS) Controller Design

An OPD analog LDO is designed to provide high gain and bandwidth for SS regulation. The proposed LDO is designed to deliver 40μA to 2.5 mA without the use of any internal capacitors to achieve stable operation. This is achieved by creating two replicas, each capable of providing up to 1.25 mA current while consuming less than 82μA quiescent current combined. The first stage of the OPD analog LDO comprises of a self-biased transconductance (gm) stage. It uses a differential pair with diode connected load transistors, as shown in fig. 8.11. To make the output node pole dominant, all the internal poles of the LDO need to be at frequencies at least 10x higher than the output pole. This is achieved by employing two separate techniques:

1) Using smaller size of the power transistor through the hybrid topology

2) Putting in a shunt buffer between the first stage and the power transistor to further push the pole at the gate of the power transistor to a higher frequency

An adaptive shunt buffer stage is inserted between the power transistor and the gm stage [62]. If the first stage is directly connected to the power transistor, the impedance at the power transistor gate is not small enough to guarantee stability with the output capaci-

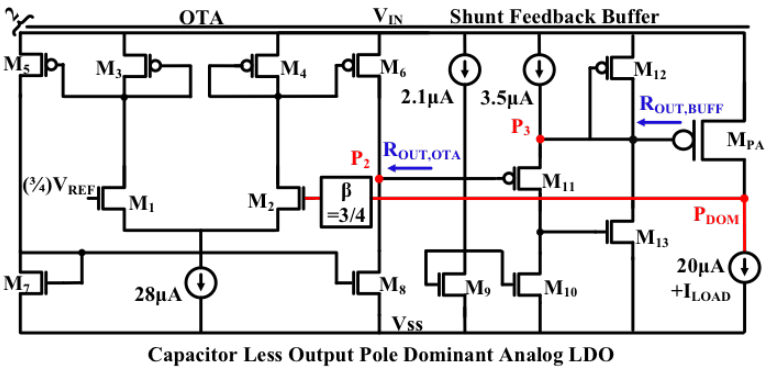


Figure 8.11: Output pole dominant (OPD) analog LDO as the SS Controller.

tance in sub-nF range. Therefore, the shunt buffer stage is used to divide this pole (second dominant) in to two high frequency poles calculated as:

$$P_2 \approx \frac{1}{2\pi R_{OUT,OTA} C_{GS,M11}} \tag{8.5}$$

$$P_3 \approx \frac{1}{2\pi R_{OUT,BUFF} C_{GS,MPA}} \approx \frac{gm_{11}(1+gm_{13})+gm_{12}}{2\pi C_{GS,MPA}} \tag{8.6}$$

P_2 is pushed to a higher frequency as the gate capacitance offered by M_{11} is very small compared to that of M_{PA}. P_3 is pushed to a higher frequency as the resistance at the gate of M_{PA} decreases due to the shunt feedback implemented through transistors M_{11}-M_{13}. M_{11} samples the voltage at the gate of the power MOS and uses M_{13} to adjust the current to complete the shunt feedback loop. Worst stability condition for the SS regulator occurs at the maximum I_{LOAD}, as the dominant output pole is at its highest possible frequency. Maintaining a high phase margin (PM) requires the shunt feedback loop to be effective when the voltage at the gate of M_{PA} has decreased to provide maximum I_{LOAD}. This is ensured by increasing the biasing current flowing through the diode-connected transistor M_{12} through the increased V_{GS}. A simulated bode plot near I_{MAX}, shown in fig. 8.12, highlights the achieved high PM at a high I_{LOAD} condition.

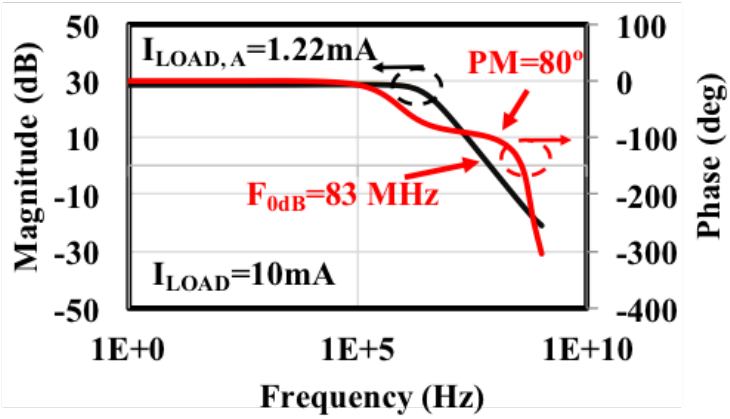


Figure 8.12: Simulated phase margin of the hybrid LDO at V_{REG}=1V.

8.5.3 Stability Analysis of the Hybrid LDO

As mentioned earlier, SS controller is designed to reject the noise in the dead-zone created by the LS controller. Small signal load regulation capacity of the SS controller is equivalent to its loop gain and bandwidth. Given the adaptive nature of the shunt feedback buffer, P_3 is the least dominant pole that adapts with changing I_{LOAD}. Therefore, loading at output of the buffer can be neglected resulting in a second order small signal loop gain for the SS controller given as:

$$LoopGain(S) \approx \frac{-0.75gm_{OUT,OTA}R_{OUT,OTA}gm_{MPA}R_{LOAD}}{(1+sR_{OUT,OTA}C_{GS,M11})(1+sR_{LOAD}C_{LOAD})} \tag{8.7}$$

The location of the P_{DOM} is directly proportional to the I_{LOAD} given as:

$$P_{DOM} \approx \frac{I_{LOAD}}{2\pi V_{LOAD}C_{LOAD}} \tag{8.8}$$

As evident from the bode plot in fig. 8.12 and fig. 8.13, the system behaves like a single pole system in the specified current range. The unity gain bandwidth ($F_{0dB,SS}$) of the SS regulator across I_{LOAD} is 10.4MHz (I_{LOAD}=20μA) and 84MHz (I_{LOAD}=10mA) and loop-gain (K_{SS}) ranges from 40dB (I_{LOAD}=10mA) to 28dB (I_{LOAD}=20μA).

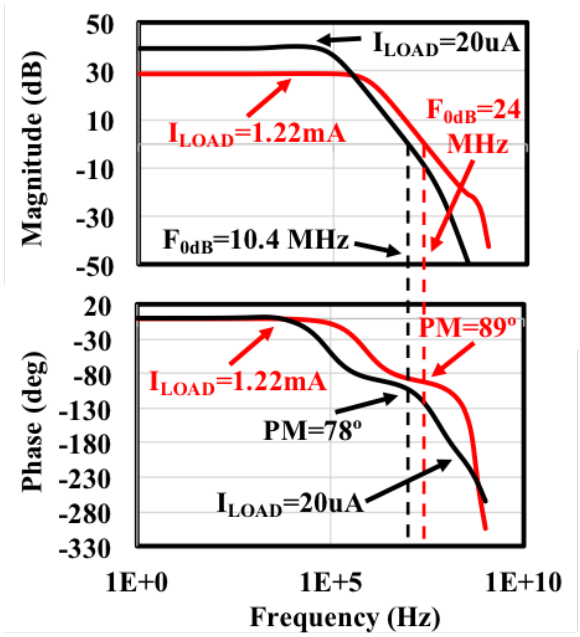
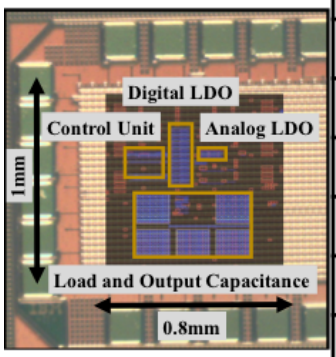


Figure 8.13: Simulated phase margin and unity gain bandwidth of the SS controller across its complete I_{LOAD} range at V_{REG}=1V.

On the other hand, the LS controller induces $F_{LCO,LS}$=46MHz and $A_{LCO,LS}$=66mV at I_{LOAD}=10mA and F_S=1GHz and $F_{LCO,LS}$=63MHz and $A_{LCO,LS}$= 25mV at I_{LOAD}=2mA and F_S=1GHz for dropout voltage of 200mV. These results are obtained through simulations when LS controller is enabled without any dead-zone with a dropout of 200mV. We observe that at I_{LOAD}=10mA, $F_{0dB,SS}$>$F_{LCO,LS}$ satisfying (8.2) and at I_{LOAD}=2mA (I_{LOAD}>single digital power transistor), $A_{LCO,LS}$<|dead-zone| satisfying (8.3). Throughout these operating conditions, I_{BIAS} of analog SS controller ensures that (8.4) is always satisfied. In case, I_{LOAD}<2mA (I_{LOAD}<single digital power transistor), and F_S=1GHz, $A_{LCO,LS}$ is less than 5mV due to the low pass filtering effect of the high operational frequency of the digital LS controller. As a result (8.3) is always satisfied resulting in stable operation of the hybrid LDO even under light load conditions (bounded by the minimum I_{LOAD} for stable operation of the SS analog controller). Thanks to the adaptive $F_{0dB,SS}$ of the SS regulator due to its output pole dominant configuration, stability constraints of SMC are always satisfied resulting in a stable operation of the proposed hybrid LDO across the complete operational



Process	GF 130nm CMOS
Package	QFN
Active Area	0.0818mm^2
V_{IN}	0.6V, 1.1-1.2V
I_{LOAD}	30µA – 12mA
V_{OUT}	0.5-0.55V, 0.8-1.1V
Load Capacitance	< 500 pF

Figure 8.14: Die micrograph with chip details.

range.

8.6 Measurement Results

Chip micrograph of the presented hybrid LDO fabricated in 130nm CMOS is shown in fig. 8.14. The LDO runs from a V_{IN} of 1.1 to 1.2 V with a dropout (V_{DO})=100-300mV and provides I_{LOAD}=12mA at a nominal V_{DO}=100mV. For V_{IN}=0.6V (NTV mode), the LDO is reconfigured to operate in a fully digital mode. It regulates for a minimum of V_{DO}=50mV and provides up to I_{LOAD}=2mA at V_{REG}=0.5V. Chattering (unstable behavior) is observed when the analog SS controller is turned off and shows accurate steady-state settling once it is enabled as shown in the scope captures of fig. 8.15. Extensive load regulation measurements (fig. 8.16) are performed across the complete operational range including hybrid and all-digital modes. The worst-case measurement showed 2.67mV/mA for I_{LOAD} up to 12mA and 3.1mV/mA for the maximum transient load step change of 10.3mA. Load regulation can be further improved by increasing the SS controller gain at maximum I_{LOAD}. A T_{RISE} and $T_{SETTLING}$ of 25ns and 45ns are measured for a load step from 30μA to 8.6mA and a $T_{SETTLING}$ of 2.8μs is measured from an overshoot generated for a load step from 8.6mA to 30μA as captured on scope in fig. 8.17. In this case, LS controller is operated at an F_S=540MHz. The hybrid LDO is turned into an all-digital LDO for V_{IN}<600mV operating

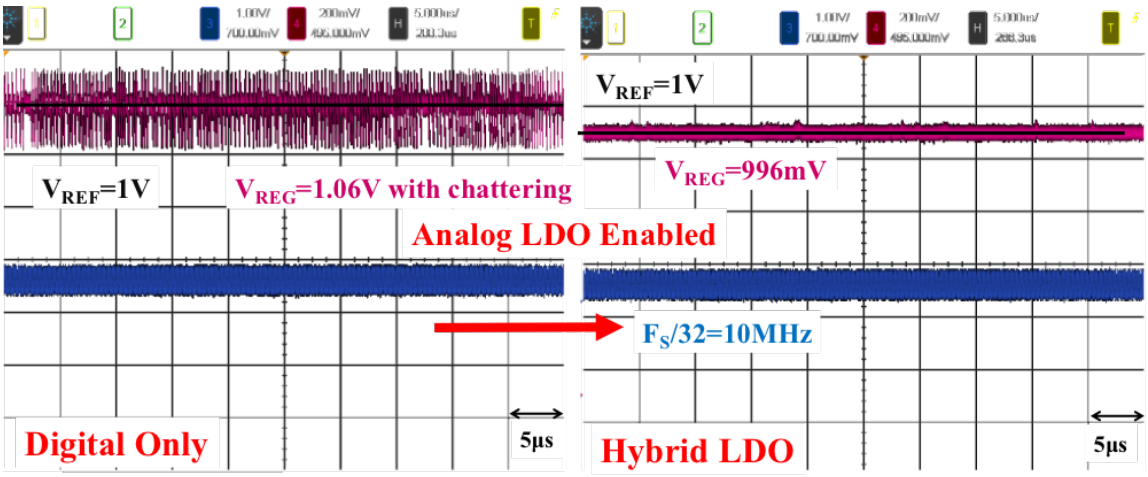


Figure 8.15: Scope capture of steady state response when SS controller is disabled and enabled.

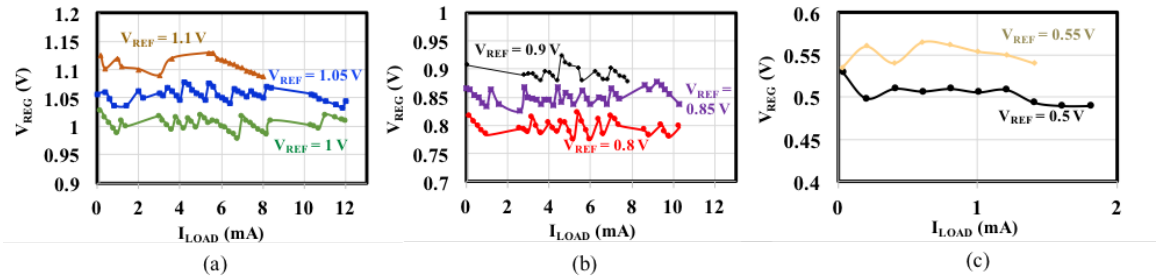


Figure 8.16: Load regulation measurements (a) with V_{IN}=1.2V (for hybrid) and (b) V_{IN}=0.6V (digital only). Worst case DC error=32mV measured at V_{REF}=0.8V.

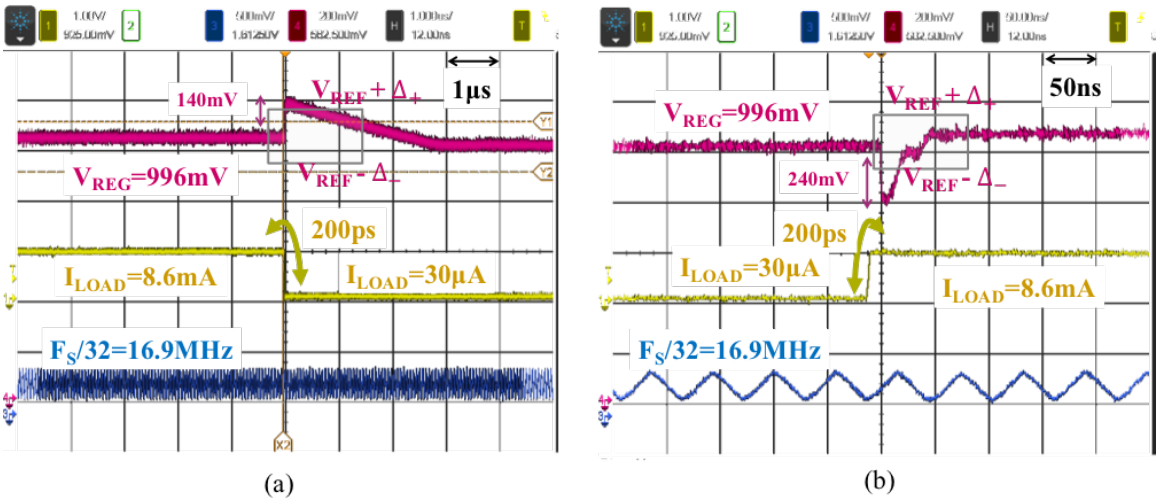


Figure 8.17: Scope capture showing hybrid LDO response to (a) I_{LOAD} step down (b) I_{LOAD} step up.

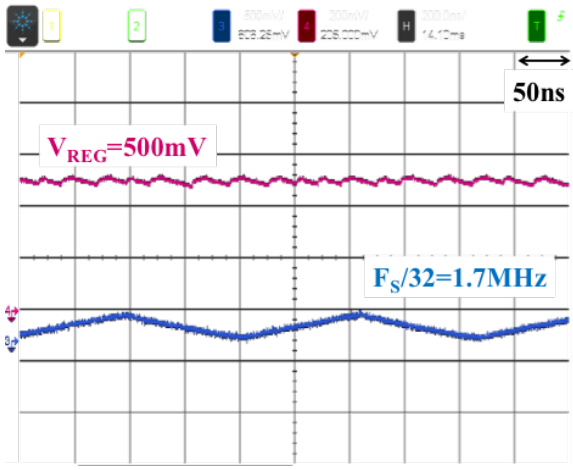


Figure 8.18: All-digital LDO configuration with V_{IN}=600mV and V_{REF}=500mV.

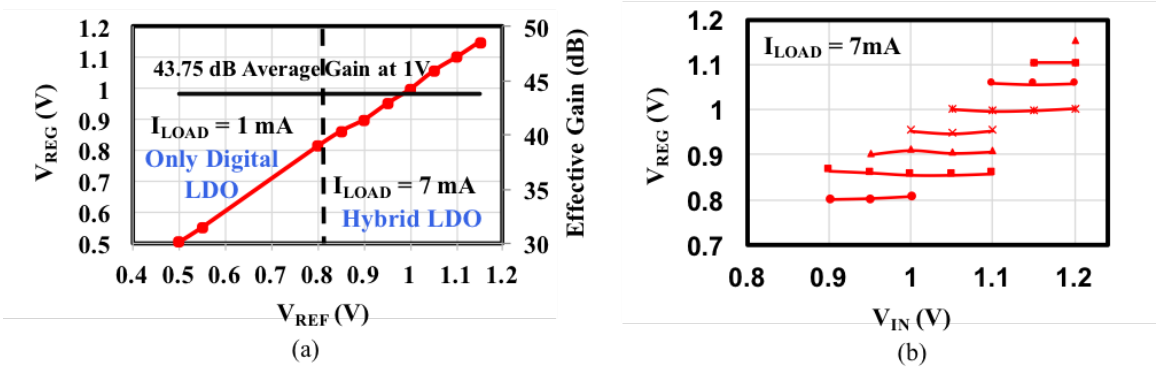


Figure 8.19: Line Regulation measurements with (a) V_{IN}=1.2V (for hybrid) and V_{IN}=0.6V (digital only) (b) with complete V_{IN} range for hybrid LDO.

at 54.4MHz. Scope capture proves regulation at V_{REF}=500mV with a small ripple as shown in fig. 8.18.

The hybrid topology exhibits high line regulation (on average <5mV error) as shown by the linearity of graph in fig. 8.19. A 43.75 dB average gain is measured at 1V from the measurements for the complete operational range of the hybrid LDO. As opposed to purely digital LDO topologies, which fail to provide considerable power supply noise rejection (PSR), the presented hybrid topology shows an average of 10-12dB PSR from 1Hz to 10MHz. As shown in fig. 8.20, the high bandwidth of the PSR graph (and the absence of PSR peaking which is typical of IPD LDOs due to degradation of the loop gain) also demonstrates the output pole dominant behavior of the designed SS controller. Scope cap-

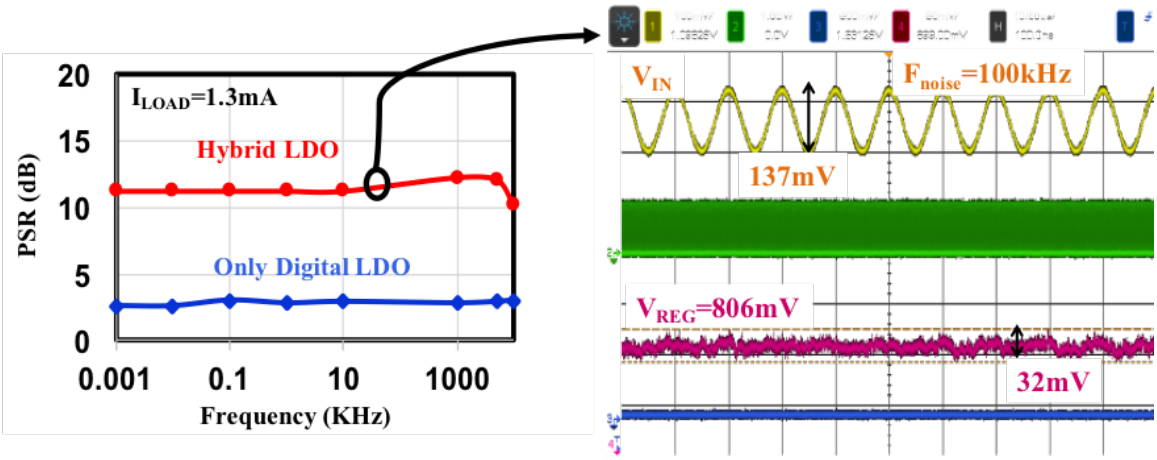


Figure 8.20: Power supply noise rejection (PSR) measurements with V_{IN}=1.2V (for hybrid), V_{IN}=0.6V(digital only) with a scope capture when F_{NOISE}=100kHz.

ture shows a PSR greater than 9dB at 100kHz (fig. 8.20). The improved PSR in the hybrid topology stems from the noise rejection capability of the analog SS controller. This is in stark contrast to an all-digital controller where we measured a nominal PSR of only 3dB.

Fig. 8.21 shows the scope capture of fast transient response both in SMC and reset SMC modes. A T_{RISE}=18ns and $T_{SETTLING}$=32ns (<2% of V_{REG}) is achieved for a load step of 30μA to 10.3mA at V_{REG}=1.05V from V_{IN}=1.2V in the SMC mode. In the reset mode, a T_{RISE}=6ns and $T_{SETTLING}$=37ns (<2% of V_{REG}) is achieved for a load step of 200μA to 8.6mA (200ps rise/fall time) at V_{REG}=1.05V from V_{IN}=1.2V. In comparison, a digital load circuit that operates for $V_{REG} \cong V_{REF}$ can resume operation after just 6ns in reset mode as compared to 18ns in SMC mode as summarized in fig. 8.22. This represents a droop recovery time of 0.71ns/mA compared to 1.74ns/mA for SMC based design. Reset mode SMC provides the best response in droop mitigation and rise time. Measurements show that SMC achieves a comparable performance to the reset mode with increasing F_S of the LS controller. In terms of settling time for V_{REG}, SMC becomes faster than the reset mode SMC as F_S of the LS controller increases (see fig. 8.23). This can be easily explained by the fact that the reset mode SMC design overcompensates the voltage droop and discharges slowly to V_{REF}. The slow discharge, however, ensures stable and smooth

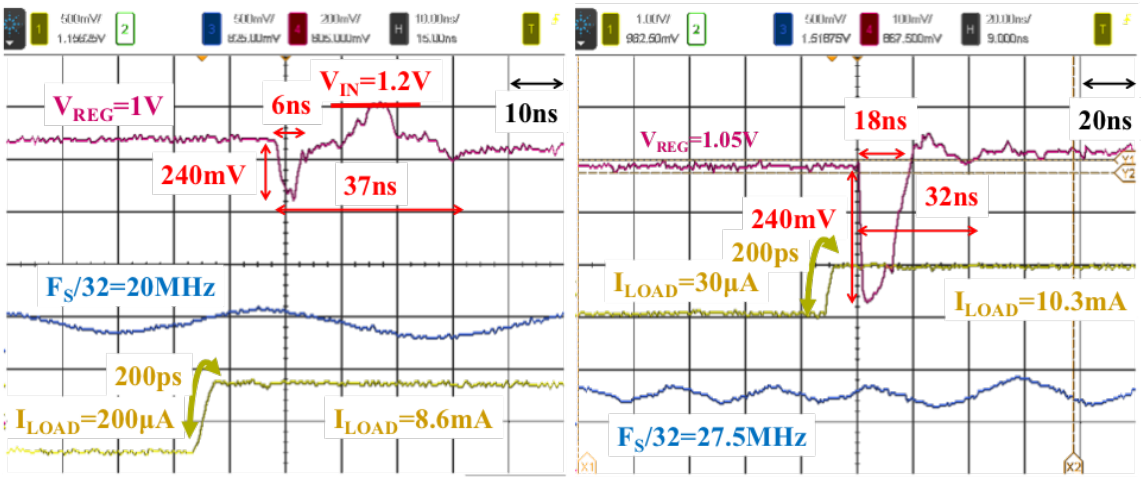


Figure 8.21: Measured operation and droop recovery for (a) Reset mode SMC (b) SMC.

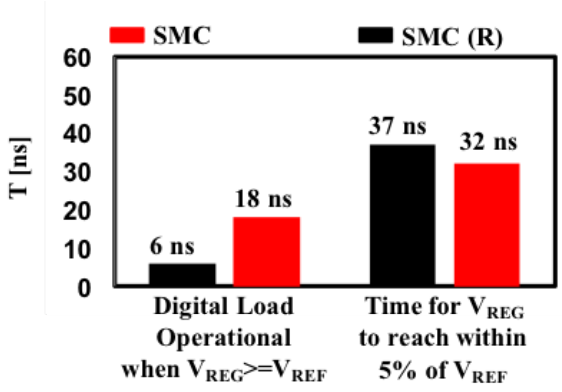


Figure 8.22: Measurements show that a faster T_{RISE} for reset SMC enables quicker resumption of operation of digital load after a droop as compared to the SMC (Digital load is assumed to operate when $V_{REG}>V_{REF}$). On the other hand, SMC shows faster $T_{SETTLING}$ as compared to the reset SMC.

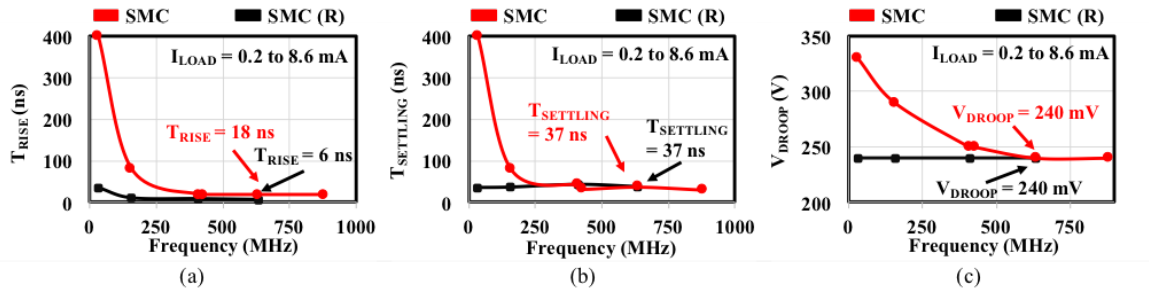


Figure 8.23: Measurements showing a comparison between boost SMC and SMC for (a) T_{RISE} (b) $T_{SETTLING}$ (c) V_{DROOP} with increasing F_S of the digital LS controller.

settling in the reset mode. A worst-case voltage droop of 240mV is measured in both reset and nominal mode at high F_S (>600MHz). The large voltage droop magnitude is attributed to the clocked comparator sampling delay, 200ps step transition in load conditions and small on-chip MOS decoupling capacitor of 500pf.

As elaborated in earlier in this chapter, in SMC, we can employ a higher LS controller FS and use adaptive bandwidth of SS controller and dead-zone to ensure that the hybrid LDO is stable. Scope captures for increasing LS controller F_S shows that V_{REG} does not undergo any oscillation between the two thresholds when $F_S \approx 138MHz$, whereas, it undergoes only a single oscillation between the two thresholds before it settles down even at a higher $F_S \approx 560MHz$. In all the scope captures of fig. 8.24 stable settling of V_{REG}=V_{REF} can be observed. As discussed in earlier, an optimal placement of the two thresholds helps achieve a near optimally damped response to transient I_{LOAD} changes. Measurements from the test-chip illustrate this and are shown in fig. 8.25. For early detection and minimization of droop, we need a $V_{REF} - \Delta_-$ closer to V_{REF}. This in turn causes larger overshoots resulting in longer $T_{SETTLING}$. We observe minimum $T_{SETTLING}$ when Δ_-=90mV. When this lower threshold is further decreased, a higher contribution from the SS regulator results in a slower response time. The measurements in this chapter are made for Δ_-=90 mV. The system shows a damped response after undergoing an overshoot, therefore, Δ_+=25mV is selected for stable response. A peak current efficiency of 98.64% is measured at I_{LOAD}=12mA and F_S=256MHz. The current efficiency curves across the complete I_{LOAD} range are shown in fig. 8.26. These measurements include all the dynamic power consumed in clock generation and distribution. Techniques like bias programming during power saving modes can be used to further improve the current efficiency of analog SS regulator. Competitive performance is achieved in transient response times and operational voltage range when compared with state-of-the-art as summarized in table 8.3.

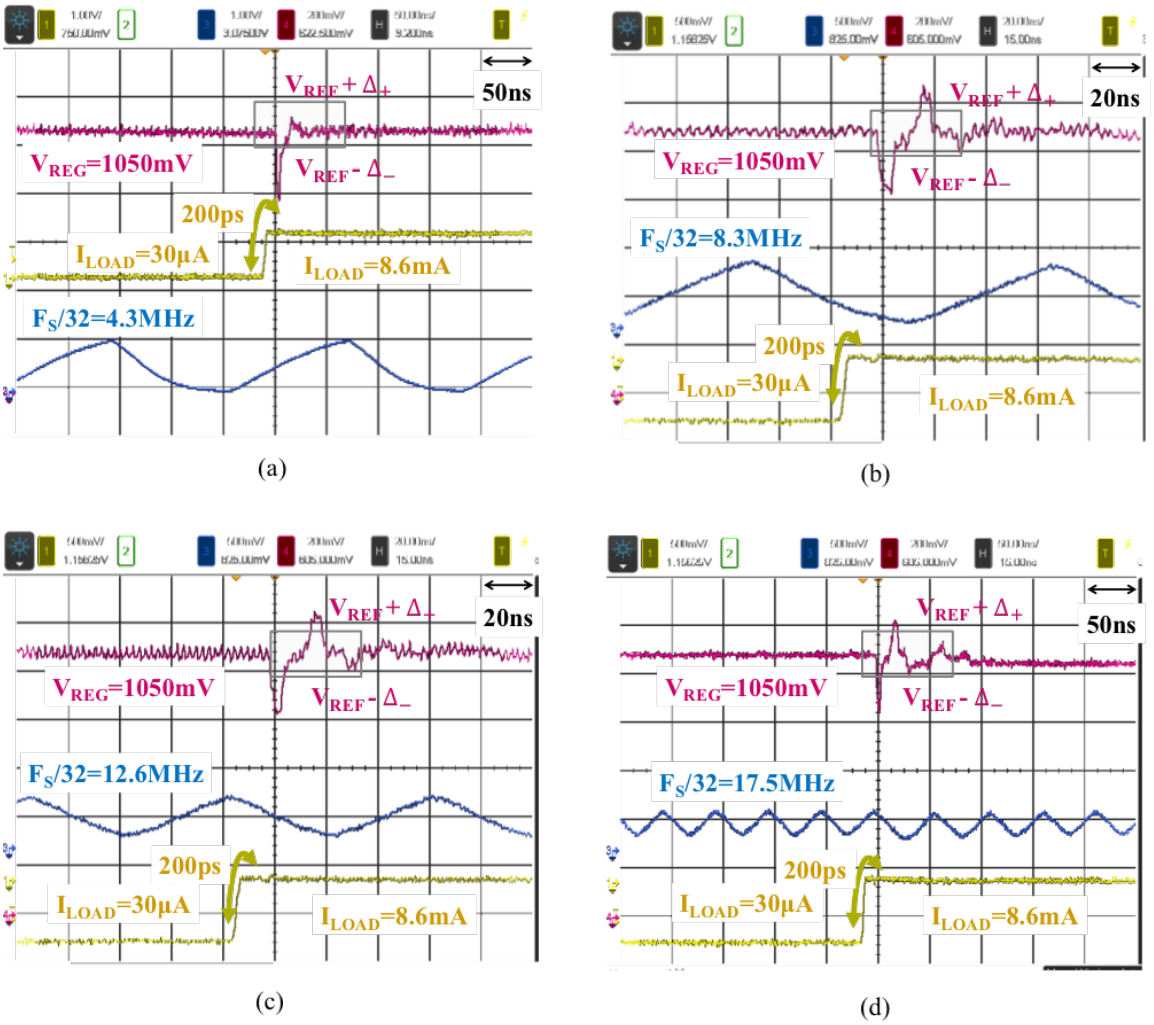


Figure 8.24: (a-d) Scope captures show that a higher F_S increases the V_{REG} excursions to the dead-zone thresholds but the gain and bandwidth of the SS controller ensures that the system settles down accurately.

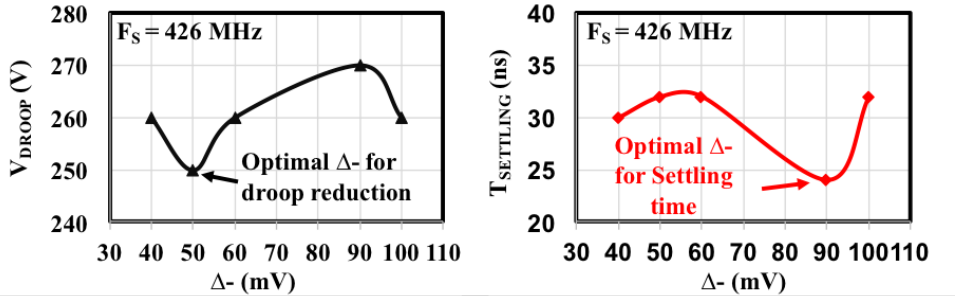


Figure 8.25: Measurements for selection of optimal Δ_- for (a) droop reduction and (b) settling time.

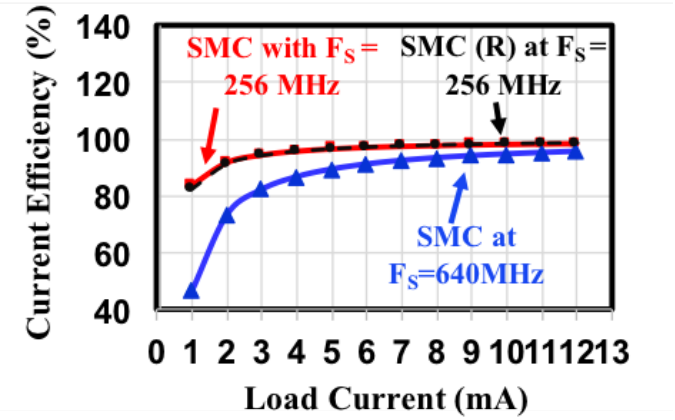


Figure 8.26: Measured current efficiency of the hybrid LDO.

Table 8.3: Comparison with state-of-the-art.

	This Work	[42]	[34]	[43]	[45]	[57]	[47]
Type	LDO	LDO	LDO	LDO	LDO	LDO	LDO
Technology	130 nm	45 nm SOI	65 nm	130 nm	65 nm	28nm	65nm
LDO Type	Digital + Analog	Multiloop	Analog	Digital	Digital	Digital	Digital
Control methodology	SMC	Linear	Linear	Adaptive	Linear	SMC like	SMC like
Control Reconfigurability	Yes	No	No	Yes	No	No	No
VIN (V)	0.6, 1.1-1.2	1.179 - 1.625	1.15	0.5 - 1.2	0.6 - 1.0	1.1	0.45-1
VOUT (V)	0.5 - 0.55, 0.8 - 1.1	0.9 - 1.1	1	0.45 - 1.14	0.55 - 0.95	0.9	0.4-0.95
Load Current: IMAX (mA)	12	42	10	4.6	500	200	0.014-3.3
Load Regulation (mV/mA)	< 2.67 @ 1V	9.8	0.15 - 0.2	< 10	0.25	NA	NA
Controller Current: ICTL(uA)	163.2	9450	50	24 - 221	300	110	8.1-258
Total Capacitance (nF)	0.5	1.46	0.14	1	1.5	23.5	100
Active Area (mm^2)	0.0818	0.075	0.0234	0.114	0.158	0.021	0.03
Peak Current Efficiency (%)	98.5 (R), 98.64 (Linear)	77.50	99.50	98.30	99.99	99.94	99.20
Droop (mV) @ Load Step (mA)	240 @ 10.3 (R)	7.6 @ 4.5	43 @ 10	40 @ 0.7	35 @ 100	120@180	34 @ 1.44
Droop recovery time (ns)	6 (R), 18 (Linear)	NA	100	300	40	NA	11200
FOM1 (ns/mA)	0.58 (R), 1.747 (Linear)	NA	10	428.5	0.4	NA	NA
FOM2 (ps)	166 (R), 244.8 (Linear)	62.4	3.01	0.0765*	1.6	7.75	20

FOM1= Droop recovery time / Load Step; FOM2= (Transient Time) * ICTL/ IMAX

NA - Insufficient data; * Normalized to technology node

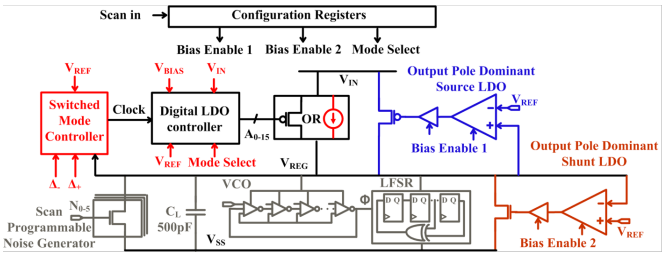
CHAPTER 9

SWITCHED-MODE-CONTROL BASED HYBRID LDO FOR ENERGY EFFICIENCY AND SUPPLY NOISE REJECTION TRADE-OFF

This thesis finally culminates by showing the usage of a hybrid LDO (using SMC) in effectively powering an analog load circuit susceptible to supply noise. It proves that a hybrid LDO built using the design concepts of both analog and digital LDOs is capable of powering any type of load circuit.

Demand for high data-rate on one hand, and high power-efficiency on the other is driving the adoption of Multi-Standard, Multi-Rate I/O (e.g. 4-32Gbps [63]) and wireless links. In these designs, the high-performance modes necessitate inclusion of low dropout regulators (LDOs) with high power supply rejection (PSR) over the entire spectrum. These LDOs use high dropouts and increased bias currents resulting in low power-efficiency numbers. On the other hand, low power modes have lower PSR requirements but are power constrained. Due to the lack of availability of LDOs with run-time programmable PSR and power-efficiency, it is a common practice to include a high PSR LDO and enable it only in the high-performance modes [63]. This results in sub-optimal performance and low power-efficiency in other modes.

To address this issue, we propose a scan-reconfigurable LDO macro that can switch between four different topologies. These topologies are based on a combination of digital and hybrid topologies discussed earlier in the thesis. They enable different PSR vs. energy-efficiency trade-offs. Key circuit blocks are shared and these blocks are enabled/disabled as required to minimize area and power overhead. Measurement results from a 130nm CMOS test-chip demonstrates wide-dynamic range of PSR from -9dB to -34dB and correlated power-efficiency of 87% to 56%, respectively. The LDO drives a ring-oscillator based voltage controlled oscillator (VCO) and a linear feedback shift register (LFSR) load



Mode	Digital	SMC	Source LDO	Shunt LDO	Design Details	PSR	Energy Efficiency
1	Linear PMOS	Disabled	Disabled	Disabled	Full Digital LDO with Linear PMOS Array	Low	Highest
2	Linear PMOS	Enabled	Enabled	Disabled	Full Digital LDO with Linear PMOS Array and Source LDO using SMC	Medium	Medium
3	Current Source	Enabled	Enabled	Disabled	Full Digital LDO with Current Source Array and Source LDO using SMC	High	Medium
4	Current Source	Enabled	Disabled	Enabled	Full Digital LDO with Current Source Array and Shunt LDO using SMC	Highest	Medium Low

Figure 9.1: Hybrid low dropout (LDO) voltage regulator design with scan reconfigurable operational modes and PSR vs energy efficiency trade-offs.

circuit. VCOs phase noise and the eye-opening at the output of the LFSR under application of supply noise are measured. It is demonstrated that the reconfigurable LDO macro can be configured to enable varying levels of PSR, which results in a minimum eye opening of 25mV/350ps and a maximum eye opening of 150mV/1.9ns under iso-supply noise ($15mV_{p\text{-}p}$) conditions.

9.1 LDO Architecture and Configuration Settings

The LDO macro leverages recent advances in energy-efficient all-digital LDOs [chapter 3], high-PSR analog LDOs [34] and switched mode control (SMC) [chapter 8]. It supports four scan programmable modes of operation (fig. 9.1) by enabling/disabling relevant circuit blocks. These four modes, their circuit implementations and key design principles are described below:

Mode-1: In mode-1, an all-digital design with an array of PMOS power MOSFETs operating in the linear region supplies the load current. A clocked comparator (F_{CLK}=10MHz) compares the output voltage (V_{REG}) with the reference (V_{REF}) and controls a shift register which turns-on/turns-off the power MOSFETs as required (fig. 9.2). This mode shows highest power-efficiency, input voltage (V_{IN}) scalability but low PSR. For an all-digital design, the F_{CLK} is set at 10MHz for the current design to meet a target limit-cycle oscillation (and hence output ripple of <5mV). Design details of the digital loop and its control settings are shown in fig. 9.2.

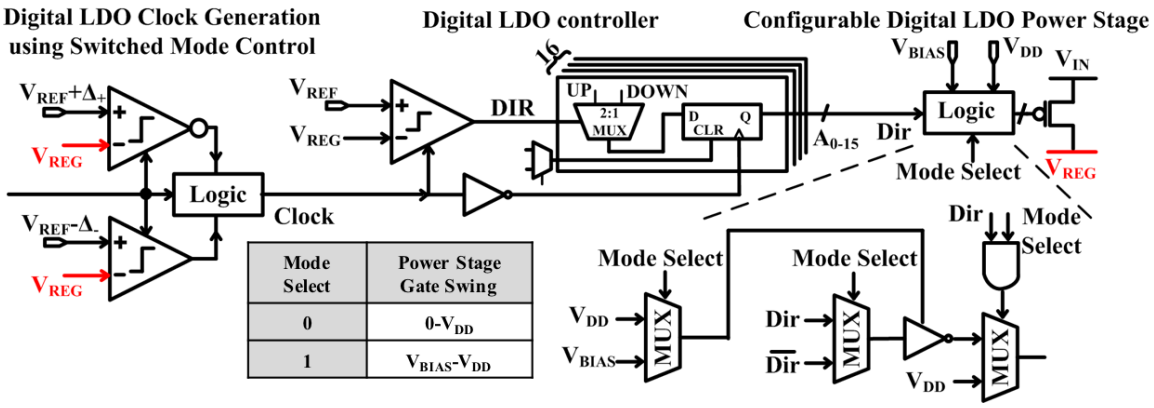


Figure 9.2: Full-digital LDO architecture with current sources/switch programmability.

Mode-2: In this mode, the digital power MOSFETs of mode-1 are supplemented with an analog LDO (source LDO) running in parallel. The source LDO supplies a part of the total load current (10-50%). The instantaneous gain of the analog loop increases the PSR at the cost of higher power. Two comparators compare V_{REG} with $V_{REF} \pm \Delta$ and run the digital LDO only when $V_{REG} < V_{REF} - \Delta_-$ or $V_{REG} > V_{REF} + \Delta_+$ via SMC (fig. 9.2). During steady-state operation only the analog LDO regulates and the digital LDO shares a part of the load current. During current transients, the digital loop is activated and provides additional current. This control topology provides:

(1) Fast transient response under load steps by turning the digital devices on/off without slew limitation and

(2) No output ripple, as the digital loop does not undergo limit cycle oscillations in the steady-state.

SMC combines the excellent small signal characteristics of an analog LDO with the high current driving capability of the digital power-MOSFETs. The digital loop is clock gated when the output voltage is within the LS dead-zone reducing the controller current.

Mode-3: In mode-3, the digital LDO power MOSFETs are reconfigured into discrete current sources running in saturation mode, by biasing their gates through mux-logic (fig. 9.2). The mux-logic either biases the gates at V_{BIAS} (mode-3) or at ground (mode-2). This topology also follows SMC configuration. In mode-3, the LDO consumes higher

bias/controller current (i.e., exhibits lower power-efficiency) but has significantly improved PSR as the discrete digital devices are biased in saturation. Because of the limited current supply from these digital devices, the total operating current range of the LDO is lower than that in mode-2.

Mode-4: The role of improved PSR is to suppress noise at the output of the LDO (V_{REG}). Apart from coupling and switching noise at supply line (V_{IN}), a significant component of line noise is self-inflicted, i.e., the load switching (di) at V_{REG} causes noise at V_{IN} (L=Package and PCB parasitic inductance). Hence, reducing noise at V_{IN} will itself lower the noise at V_{REG}, and will add to an increased PSR of the LDO. In mode-4, we address this issue by

(1) Supplying constant current through discrete current sources from V_{IN} to V_{REG} and

(2) regulating V_{REG} with an NMOS LDO operating in shunt with the load in SMC configuration.

This topology:

(1) reduces V_{REG} noise through the high PSR shunt LDO and

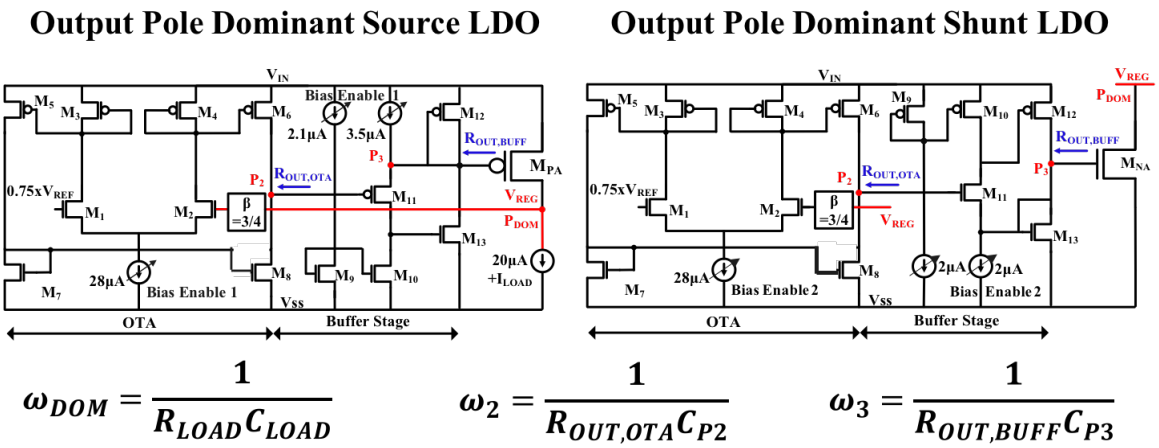
(2) eliminates self-injected noise at V_{IN}.

The shunt LDO consumes 15-20% (depending on the work-load) of the load current (see fig. 9.4) and provides the highest noise rejection at the cost of power-efficiency.

Critical circuit blocks, including the error amplifiers, biasing arms, digital power devices, scan blocks are shared among the four modes to minimize area and power (leakage) overhead. The reconfigurable macro supports scan-programmable load-transistors with high-speed droop generation and an LFSR circuit running on a ring oscillator based VCO (fig. 9.1).

9.2 Design of the analog regulation loops

The load sharing between discrete devices (in linear for mode-2 or saturation for mode-3) and the analog loop (source for mode-2 and mode-3 or shunt for mode-4) reduces the



$$\omega_{DOM} = \frac{1}{R_{LOAD}C_{LOAD}} \qquad \omega_2 = \frac{1}{R_{OUT,OTA}C_{P2}} \qquad \omega_3 = \frac{1}{R_{OUT,BUFF}C_{P3}}$$

Figure 9.3: Design schematic of output pole dominant analog voltage regulators acting as source and shunt LDOs.

current demand on the analog part. While the digital devices provide most of the DC current, the analog loop provides the dynamic current. This current (15-20% of the total load current) can be delivered by a smaller power PMOS (source LDO) or NMOS (shunt LDO) resulting in a smaller internal capacitor at the gate of the power MOSFETs. A shunt buffer between an operational trans-conductance amplifier (OTA) and the power MOSFETs (fig. 9.3) further pushes the internal poles to even higher frequencies. This results in the output pole of the LDO being dominant with only 500pf (at 1V) on-die MOS capacitor without requiring any external capacitor. This topology shows:

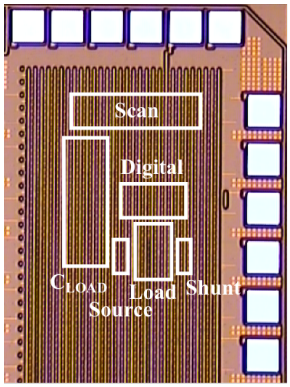
(1) High transient bandwidth with full spectrum noise rejection

(2) No PSR peaking, which is a typical challenge for conventional internal pole dominant analog LDOs [64, 65].

The design of the source LDO (mode-2 and mode-3) is same as in chapter 8 and the shunt LDO features a complementary design.

9.3 Measurement Results

The test-chip is fabricated in GF 130nm CMOS (see fig. 9.4). The maximum load current that can be delivered decreases as discrete devices are biased as current sources (mode-3)



Technology	130nm CMOS
LDO Active Area	0.0167 mm^2
C_{LOAD}	500 pF
Testing Interface	32 Pin QFN Package

Mode	V_{IN} (V)	V_{REG} (V)	I_{CNTL} (mA)	$I_{LOAD,MAX}$ (mA)
1	1.2-0.65	0.8-0.55	0.057	5
2	1.2-0.96	0.8-0.7	0.124	5
3	1.2-1.15	0.8-0.7	0.146	4.7
4	1.2	0.8	0.240	1.4

Figure 9.4: Chip micrograph with test interface and operational range of the LDO macro in different modes

and further when the shunt LDO is activated (mode-4). Correspondingly, the bias/controller current increases from mode-1 to mode-4. This results in decreasing current efficiency from mode-1 to mode-4. The minimum dropout increases from mode-1 (80mV) to mode-4 (400mV). Thus, we observe a monotonic increase of current and power efficiency as the LDO is reconfigured from mode-4 to mode-1. The plot of PSR vs frequency in fig. 9.5 (measured with $80mV_{p\text{-}p}$ injected input noise at V_{IN}) demonstrates:

(1) Programmable and increasing PSR from mode-1 (-9dB at 100MHz) to mode-4 (-34dB at 100MHz)

(2) PSR improvement from mode-3 to mode-4 through reduction of self-induced noise at V_{IN}

(3) High PSR bandwidth and no PSR peaking, consistent with an output pole dominant LDO loop.

To understand the efficacy of this design, we measure the performance of the LFSR and VCO circuits (fig. 9.6 and fig. 9.7) under $15mV_{p\text{-}p}$ input line noise (at V_{IN}). Oscilloscope captures of the LFSRs output running at 420MHz shows an increasing eye-opening for

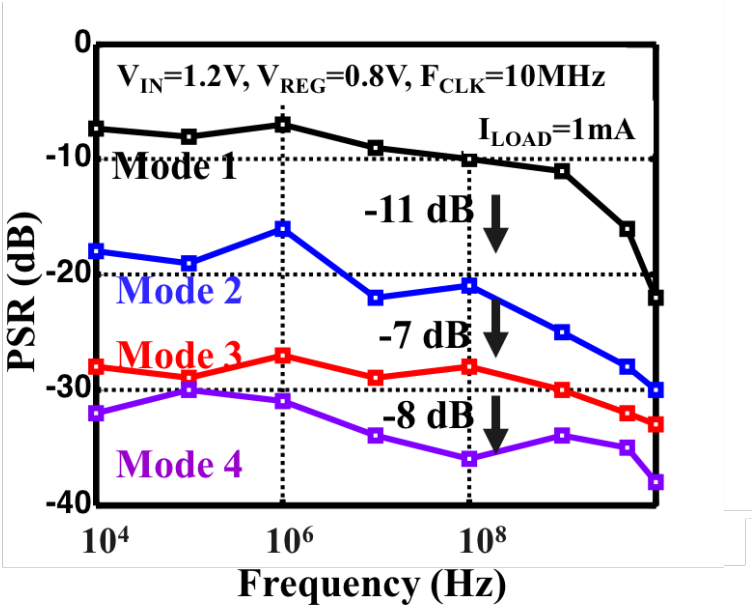


Figure 9.5: Measured PSR.

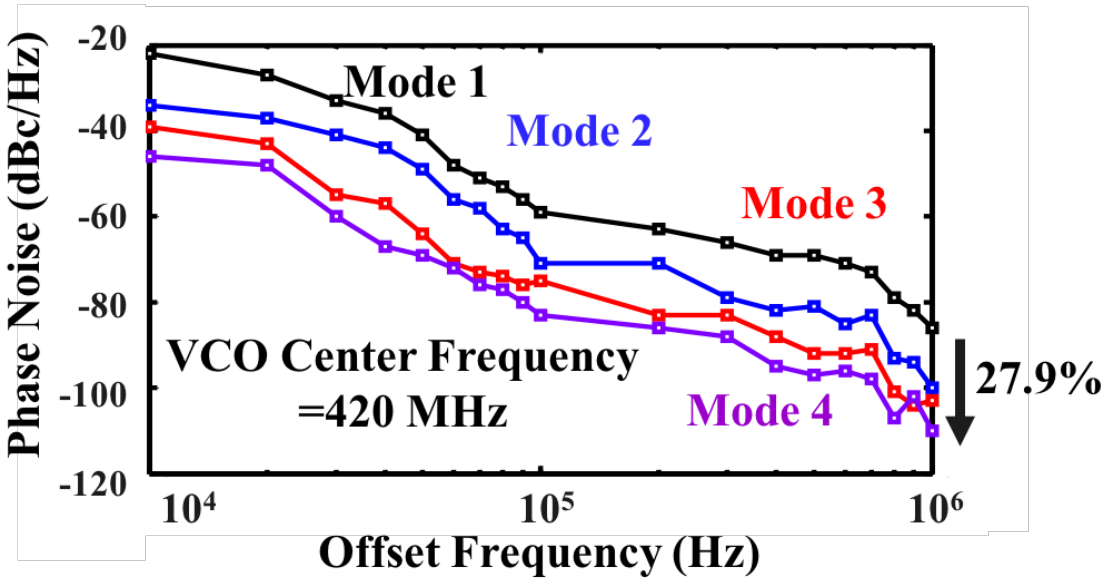


Figure 9.6: Measured phase noise of the designed VCO is shown. Measurements with 15m$V_{p\text{-}p}$ ripple at 100 MHz on the supply.

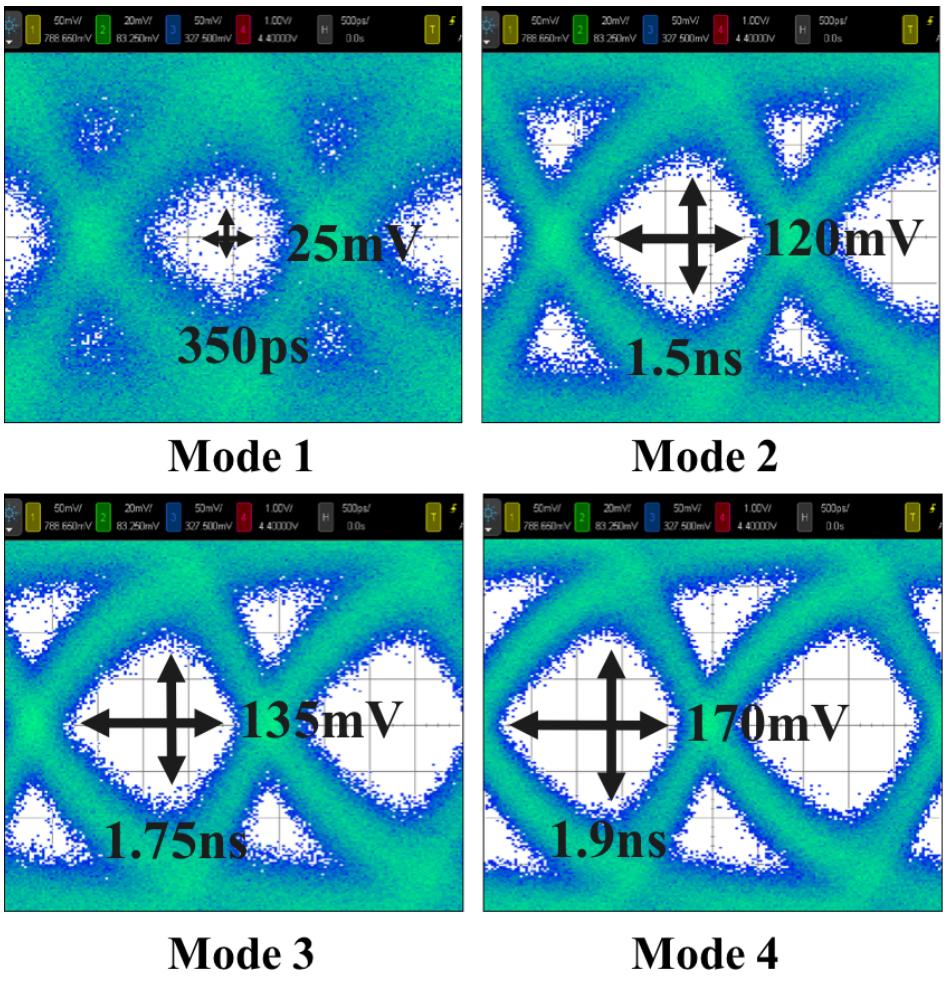
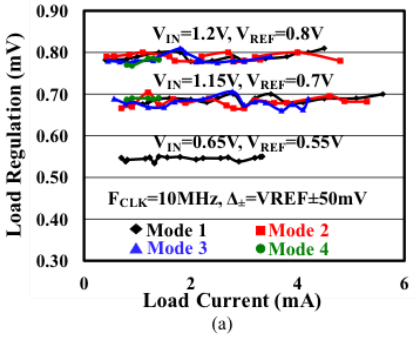
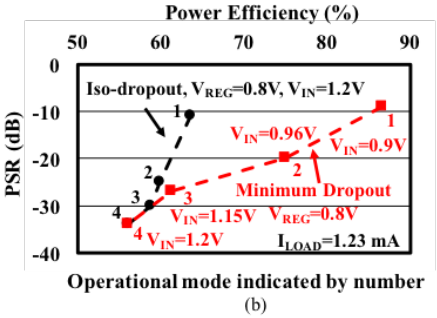


Figure 9.7: Measured LFSR eye plots, generated using 1000 cycles and 15mVpp ripple on the supply, show the gradual performance improvement from mode 1 to mode 4.

1000 cycles from mode-1 (25mV/350ps) to mode-4 (150mV/1.9ns). The single side-band phase noise of the free-running VCO illustrates 27.9% improvement at 1MHz from mode-1 to mode-4. It should be noted that the phase noise measurements were performed with injected noise at V_{IN} as well as switching load at V_{REG}. This captures the true phase noise when a digital load circuit operating on a shared V_{IN} injects switching noise to the supply. Measured load regulation is shown in fig. 9.8a.

The LDO macro provides a wide range of PSR and power-efficiency. PSR/power-efficiency is measured for iso-dropout (V_{IN}=1.2V and V_{REG}=0.8V) as well as for the minimum dropout (at V_{REG}=0.8V) that can be supported in each mode. From mode-1 to mode-4,





Mode	Total Area (mm^2)	Area Overhead
1	0.0140	1x
2	0.0153	1.096x
3	0.0267	1.909x
4	0.0261	1.867x

(c)

Figure 9.8: (a) Measured load regulation across the complete operational range shows high DC accuracy. (b) A programmable range of 23dB PSR is measured with a change of 35.6% power efficiency. (c) Shows the silicon area trade-off for different modes of operation.

Table 9.1: Comparison with state-of-the-art.

Parameter	This Work	[63]	[34]	[43]
Technology	130nm CMOS	22 nm CMOS	65nm CMOS	130 nm CMOS
LDO Type	Digital, Hybrid	Hybrid	Analog	Digital
Reconfiguration	Yes	No		
PSR (dB)	-9 to -34	-30	-22.5	NA
Reconfiguration Range	PSR (3.7X), η (1.55X)	No reconfiguration range		
Peak Current Efficiency	99.43	85-90	99.5	98.3
FOM= Peak Linear |PSR|* x η	43.6	25.36	11.05	NA

η=Peak Power Efficiency, * Linear |PSR|=ΔVIN/ΔVREG

the PSR increases monotonically (peak PSR is -34dB at 100MHz), in a manner that cannot be otherwise realized by using a single controller and changing biasing conditions or dropout voltages. Within each mode, we observe increasing PSR with increasing dropout thus providing the flexibility of selecting a desired PSR. Correlated with decreasing PSR is an increase in power-efficiency as the macro is reconfigured. Peak power-efficiency of 87% (mode-1), 75% (mode-2), 61% (mode-3) and 56% (mode-4) are measured. Fig. 9.8b illustrates the wide range of PSR and energy-efficiency trade-off that is offered by the scan programmable LDO macro. Area overhead for each mode normalized to mode-1 is compared in fig. 9.8c. Comparison with state-of-the-art static designs in Table 9.1 show competitive metrics.

CHAPTER 10
CONCLUSION

With decreasing transistor size, routing metal geometry and supply voltage delivering high fidelity power right at the point of load inside a chip has become difficult. This problem is further exacerbated by the wide dynamic range and heterogeneous load circuits which exhibit multiple power and performance modes. To address this challenge of supplying high fidelity power supply right at the point of load in big microprocessor and system-on-chip platforms, this dissertation research proposes digital and digitally-assisted linear voltage regulators. These linear voltage regulators can be embedded right at the point of load thanks to their digital synthesis, small footprint, low power overhead and inbuilt performance adaptation.

This thesis research contributes towards understanding the transient and steady-state operational dynamics of synchronous digital LDOs. A z-domain model is used to analyze the stability and transient performance of a baseline digital LDO. To understand the steady-state dynamics a describing function based pseudo linear model is devised. These models proved that an increase in operational clock frequency improves transient performance but can result in unstable behaviour and limit cycle oscillations. Based on these theoretical insights, a first of its kind digital LDO employing adaptive control is built in 130nm CMOS process to achieve a wide operational range compared to its predecessors.

A digital LDO suffers from low power supply noise rejection (PSR) capacity because its power transistors are operated as on/off switches. In this thesis research, PSR of the digital LDO topology is modeled and control knobs are identified to improve it proactively against supply noise paving the way to employ digital LDOs for noise sensitive load circuits. This design is also proved experimentally by designing a proactive digital LDO in 130nm CMOS process. Research on digital LDO in this thesis culminates with the design of a large load

current capacity digital LDO capable of powering a core-scale digital circuit. Building on the insights from prior designs, this design decouples the transient response of the digital LDO from its steady-state performance by employing asynchronous non-linear control. A current efficiency of greater than 99.99% is achieved with fast transient response in a test-chip built in 65nm CMOS process improving state-of-the-art in on-chip power management using digital LDOs.

To achieve load circuit agnostic voltage regulation using a digital LDO, a hybrid LDO structure is designed as a part of this thesis research. It is a first of its kind hybrid LDO that combines the fast transient performance of a digital LDO with accurate steady-state dynamics of an analog LDO utilizing switched-mode-control. Theoretical stability modeling of this hybrid LDO is devised allowing the designers to ensure stability during design phase. This theoretical model builds on small-gain theorem and can be applied to other dual-loop digital LDOs that are being pursued by the research community. A test-chip featuring this design is built in 130nm CMOS process which showed best-in-class transient performance at the time of its publication and smooth ripple-free steady-state dynamics. Utilizing the infrastructure developed in digital and hybrid LDO research, another reconfigurable hybrid LDO macro is built in 130nm to achieve a wide range of energy efficiency and PSR trade-off for wire-line I/O applications. This design can be reconfigured to analog, digital and hybrid configurations depending on the load circuit requirement and occupies a very small silicon real estate. Application of this LDO to wire-line circuits shows its adaptability to be employed for voltage regulation of wide dynamic range and noise sensitive load circuits.

This thesis research has spawned newer LDO topologies and developed generic theoretical guidelines to not only build but also model newer LDO topologies following digital or hybrid design fundamentals. Given their ease of design, the digital and digitally-assisted linear voltage regulator topologies presented in this thesis research can be embedded deep inside a big-chip in numbers to realize a true fine-grain power management setup. The author has explored this research vector and believes it is worth pursuing to achieve another

magnitude of energy savings and increased performance. Similarly, minimizing voltage conversion stages between the AC supply and the on-chip power delivery network can also add further to the possible energy savings.

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